

Model Name : Jimny_RBH / Ignis_RBH
Compal Project Name : HH51R

Compal Confidential

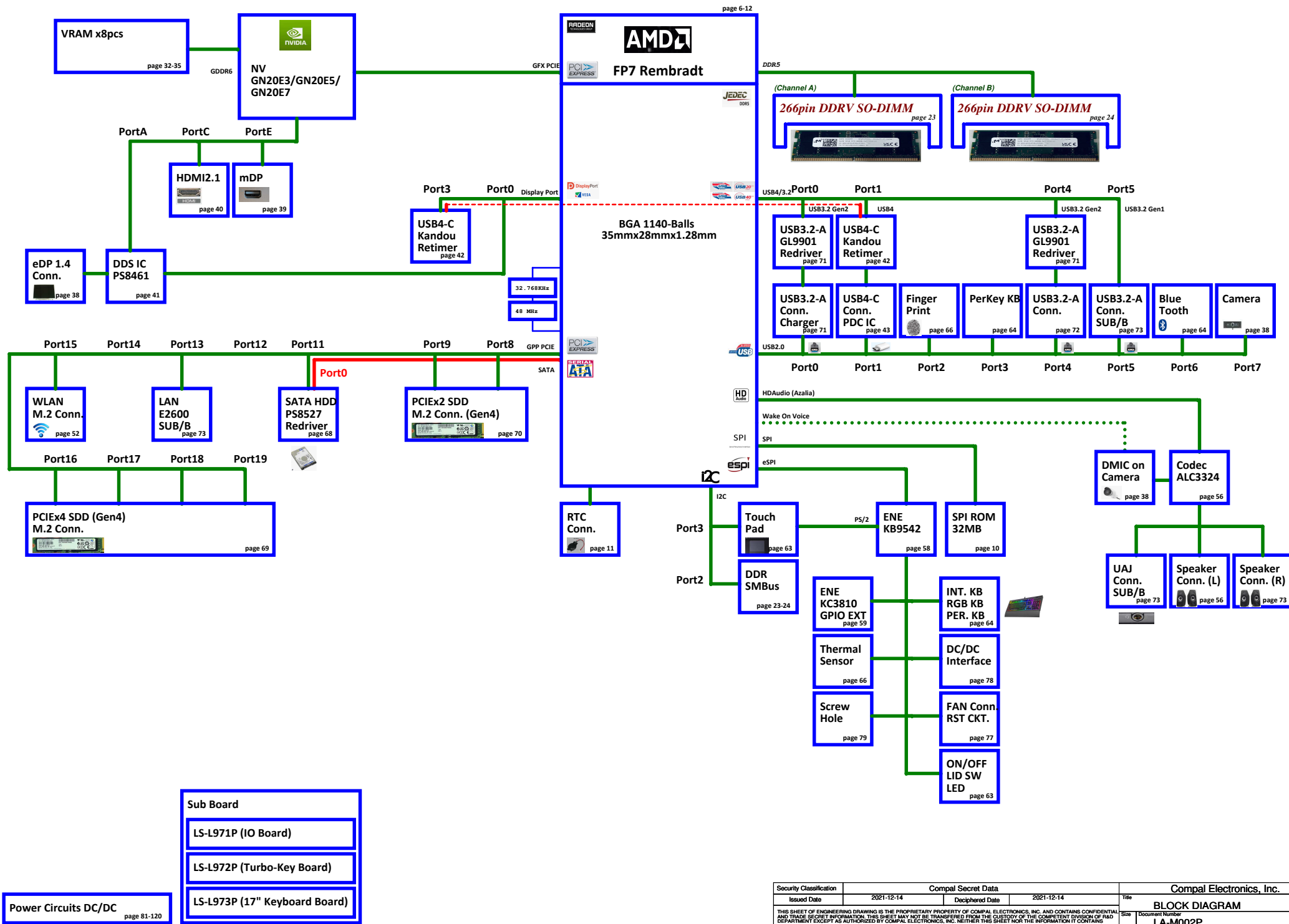
MB Schematics Document

AMD Rembrandt Platform

LA-M002P REV: 1A

2022-01-26

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








Voltage Rails

Power Plane	Description	S0	S3/MS	S5
+19VB	AC or DC Power Rail Supply	ON	ON	ON
+RTC_BATT	RTC Coin Battery Voltage	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	AC-ON DC-OFF
+3VALW	3.3V always on power rail	ON	ON	OFF
+1.8VALW	1.8V always on power rail	ON	ON	OFF
+0.75VALW	0.75V always on power rail	ON	ON	OFF
+5VALW_DDR1 +5VALW_DDR2	5V Power Rail for SO-DIMM DDR5	ON	ON	OFF
+1.1V	1.1V Power Rail for APU	ON	ON	OFF
+0.78V	0.78V Power Rail for APU	ON	ON	OFF
+VDDCR_VDD	APU Core Voltage	ON	OFF	OFF
+VDDCR_SOC	APU Core SOC Volatge	ON	OFF	OFF
+VDDCR_SR	APU Core SR Volatge	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail	ON	OFF	OFF
Power Plane On Devices	Description	S0	S3/MS	S5
+3VLP_PD	3.3V Power Rail for PD Controller	ON	ON	ON
+3V_U4RD	3.3V Power Rail for USB4 Retimer	ON	ON	OFF
+VDDIO_AUDIO	1.8V Power Rail for APU Audio I/O	ON	ON	OFF
+VDDA	5V Power Rail for Codec	ON	ON	OFF
+DMIC_VCC	1.8V Power Rail for DMIC	ON	ON	OFF
+USB3_VCCA	5V Power Rail for USB-A	ON	ON	OFF
+USB3_VCCB	5V Power Rail for USB-A	ON	ON	OFF
+3V_WLAN	3.3V Power Rail for WLAN	ON	ON	OFF
+3V_LAN	3.3V Power Rail for LAN	ON	ON	OFF
+TP_VCC	3.3V Power Rail for Touch Pad	ON	ON	OFF
+FP_VCC	3.3V Power Rail for Finger Print	ON	ON	OFF
+5V_HDD	5V Power Rail for HDD	ON	OFF	OFF
+LCDVDD	3.3V Power Rail for LCD Panel	ON	OFF	OFF
+5V_PERKEY	5V Power Rail for Perkey KeyBoard	ON	OFF	OFF
+5V_LOGO	5V Power Rail for LOGO Light Conn.	ON	OFF	OFF
+5V_LBAR	5V Power Rail for Light Bar Conn.	ON	OFF	OFF
+5VS_BL	5V Power Rail for KeyBoard Back Light	ON	OFF	OFF
+3VS_SSD1	3.3V Power Rail for SSD1 Conn.	ON	OFF	OFF
+3VS_SSD2	3.3V Power Rail for SSD2 Conn.	ON	OFF	OFF

APU SMBus/I2C Address Table

Master	Device	Address[7:1]	Address[7:0]W	Address[7:0]R
I2C Port 0 (+1.8VS)				
I2C Port 1 (+1.8VS)				
I2C Port 2 (+1.8VS) SMBus Port 0 (+1.8VS)	JDIMM1 JDIMM2	0101 0000b 50h 0101 0001b 51h	1010 0000b A0h 1010 0010b A2h	1010 0001b A1h 1010 0011b A3h
I2C Port 3 (+1.8VALW) SMBus Port 1 (+1.8VALW)	PTP (Synaptics) PTP (ELAN)	0010 1100b 2Ch 0011 1111b 19h	0101 1000b 50h 0011 1110b 3Eh	0101 1001b 50h 0011 1111b 3Fh

Board ID / SKU ID Table for AD channel

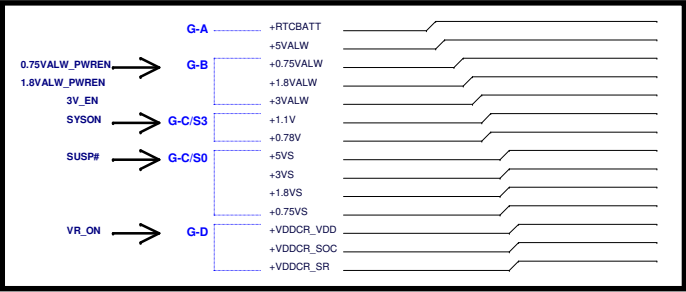
EC Borad ID	Rb
6 50/60 RVT	 R778 0 0402 2% VTD @ SD002000000
1 50 DVT Nocrml Keyboard	 R778 12K 0402 1% SD0VTD @ SD0034120200
2 50 PVT Nocrml Keyboard	 R778 15K 0402 1% SD0PVT @ SD0034150200
3 50 HP Nocrml Keyboard	 R778 20K 0402 1% SD0HP @ SD0034200200
4	 R778 27K 0402 1% @ SD0034270200
5 50 DVT RGB Keyboard	 R778 33K 0402 1% SD0VTRGB @ SD0034330200
6 50 PVT RGB Keyboard	 R778 43K 0402 1% SD0PVRGB @ SD0034430200
7 50 HP RGB Keyboard	 R778 56K 0402 1% SD0HPRGB @ SD0034560200
9 60 DVT Nocrml Keyboard	 R778 100K 0402 1% SD0VTD @ SD0034100200
10 60 PVT Nocrml Keyboard	 R778 130K 0402 1% SD0PVT @ SD0034130200
11 60 HP Nocrml Keyboard	 R778 160K 0402 1% SD0HP @ SD0034200200
12	 R778 200K 0402 1% @ SD0034200200
13 60 DVT RGB Keyboard	 R778 240K 0402 1% SD0VTRGB @ SD0000001800
14 60 PVT RGB Keyboard	 R778 270K 0402 1% SD0PVRGB @ SD0000000200
15	 R778 330K 0402 1% @ SD0034330200
16	 R778 430K 0402 1% @ SD000000W000
17	 R778 560K 0402 1% @ SD0034560200
18 60 HP RGB Keyboard	 R778 750K 0402 1% SD0HPRGB @ SD000000AL 60
19	Unpop

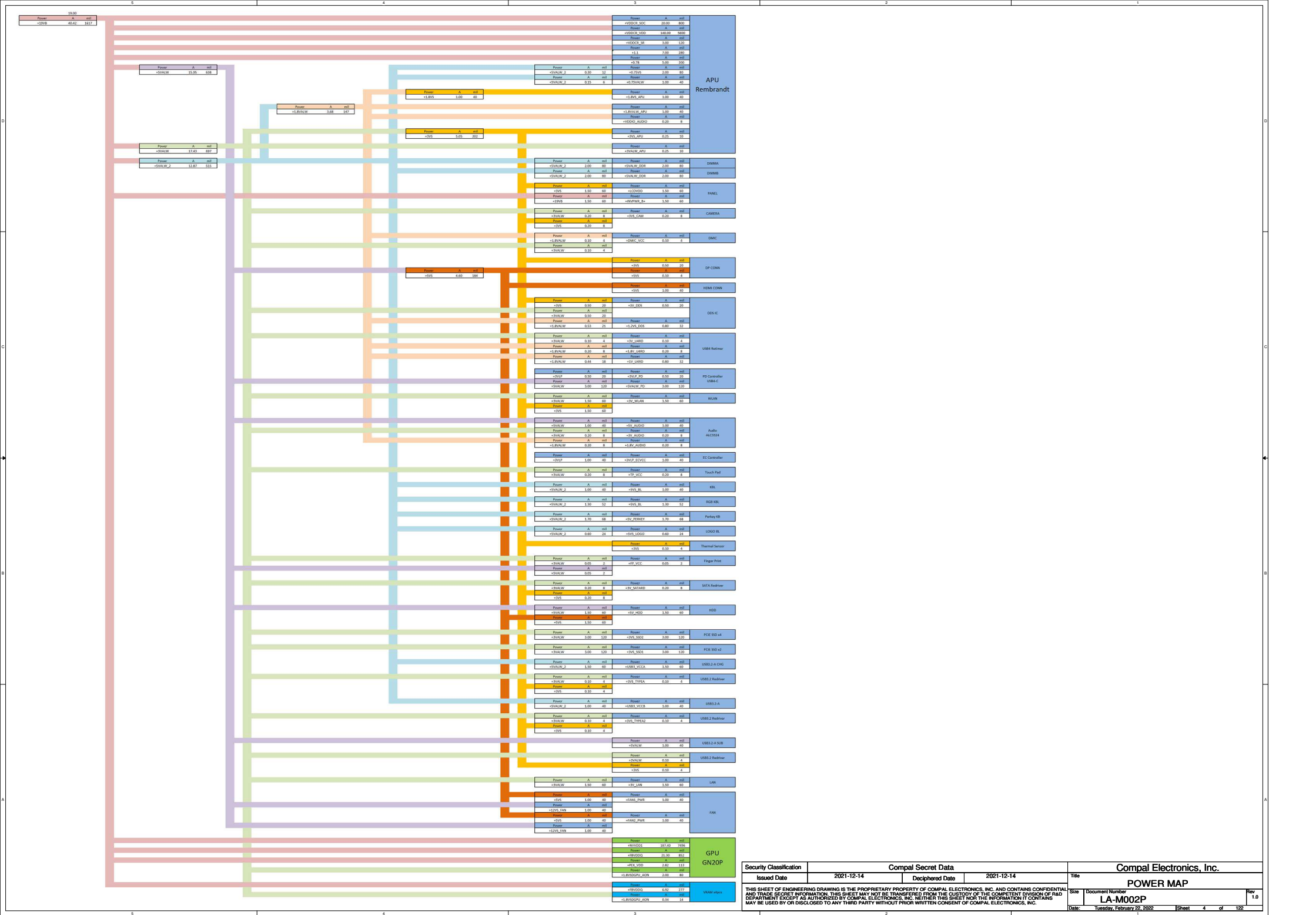
Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb	V min	V typ	V max	EC AD
6	0	0.000V	0.300V	0x00 - 0x0B	
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.414V	1.430V	1.446V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xA8 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.910V	2.919V	0xDD - 0xEE
19	MC	3.000V	3.300V	3.500V	0xEF - 0xFF

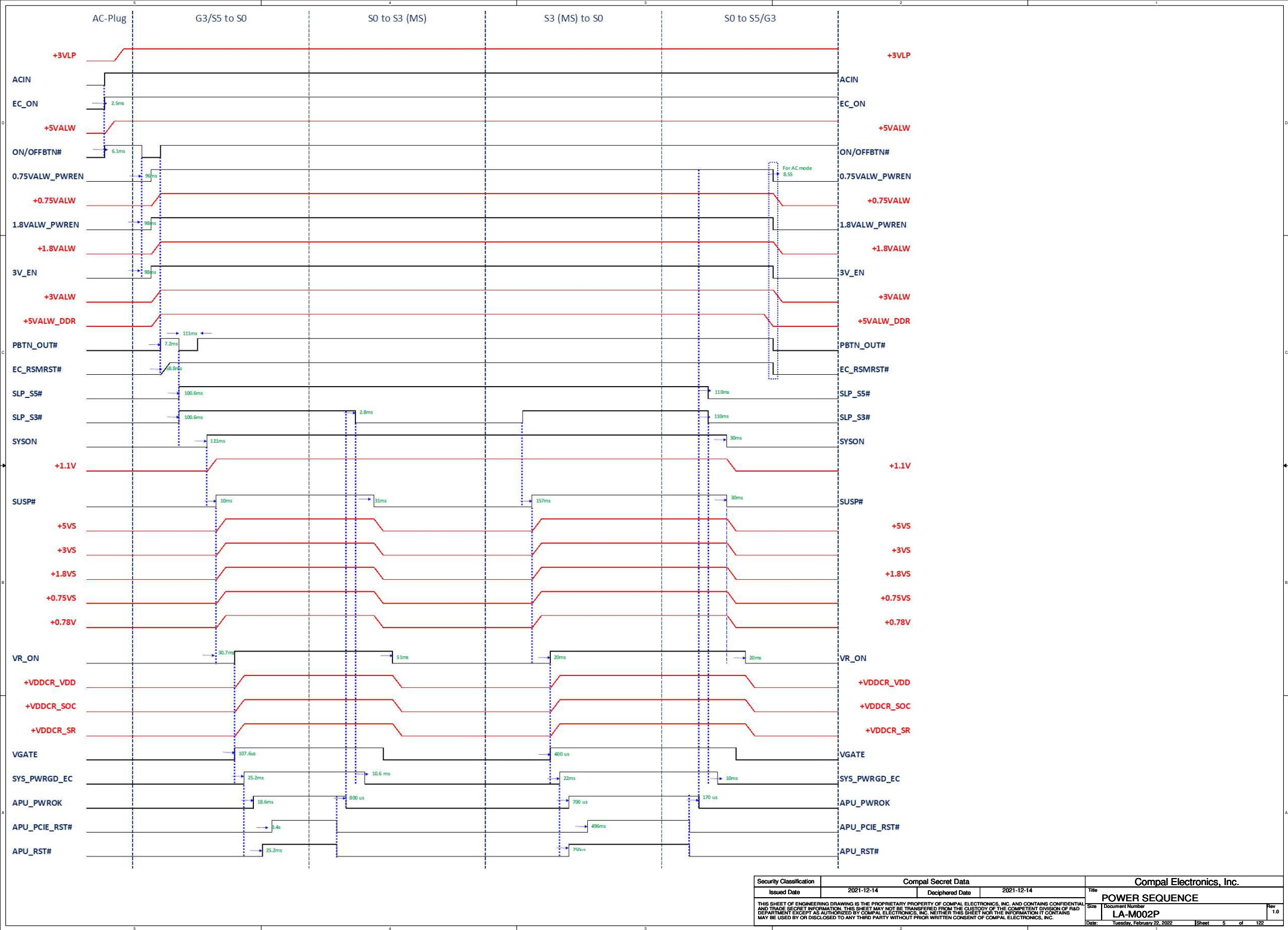
BOM Structure Table

BOM Structure	Description
@/DR@	Components Do Not Install/Design Reserve Components
45@/TP@/PCB@	HDMI Royalty PN/Test Point/PCB PN
CONN@/JP@/RS@	Mechanical Connector/Jump/R-Short
HDT@	AMD HDT Debug Components
TMS@/TMSIEC@	Thermal sensor /Thermal sensor for IEC
CHG@/CW@/SLG@	USB Charger/CeWell/Sligro
HDD@	HDD Components including SATA Redriver
LED14P@	RGB Keyboard
VGA@/GC6@	VGA/GC6 Components
12VGPU@/5VGPU@/12VCPUP@/5VCPUP@	12V FAN & 5V FAN
EMI@/@EMI@	EMI Components Install/Uninstall
ESD@/@ESD@	ESD Components Install/Uninstall
FP@	Finger Print Components
DP@	Mini Display Port Components
EVT@/DVT@/MP@ EVTRGB@/DVTRGB@/MPRGB@	EC FW Board ID
LOGO@/LB@/TURBO@	LOGO Light/Light Bar/Turbo Key Components
PERKEY@/EMIPERKEY@	Perkey KeyBoard Components install
KB@	KeyBoard Components
ECEXT1@/ECEXT2@	EC GPIO EXTEND 1/2 Components
RF@/@RF@	RF Components Install/Uninstall
OVRM@/GEN1@/GEN2@	OVRM Gen1/Gen2 Components
uPI_GEN1@/uPI_GEN2@	OVRM uPI Gen1/Gen2 Components
ON_GEN1@/ON_GEN2@	OVRM ON Gen1/Gen2 Components
ON_80W_GEN1@/ON_100W_GEN1@	OVRM ON Gen1 80W/100W Components
uPI_80W_GEN1@/uPI_100W_GEN1@	OVRM uPI Gen1 80W/100W Components
MAXP@/MAXQ@/RBH@/RBU@	APU GPIO Strap Pin Clonfig
X76VSAM8@/X76VSAM@	Samsung VRAM 8Gb/6Gb Components
X76VHYN8@/X76VHYN@	Hynix VRAM 8Gb/6Gb Components
X76V16G@	Samsung VRAM 16Gb Components
QN20E1@/QN20E5@	QN20 Series GPU PN
GN20P1B@/GN20E3@/GN20E5@/GN20E7@	GN20 Series GPU PN
GSYNC@/NGSYNC@	G-Sync/Non G-Sync Support
518@/532@	APU PN
ALC3324@/ALC287@	Audio IC PN
DDSA2@/DDSA3@	DDS IC A2/A3 version Components

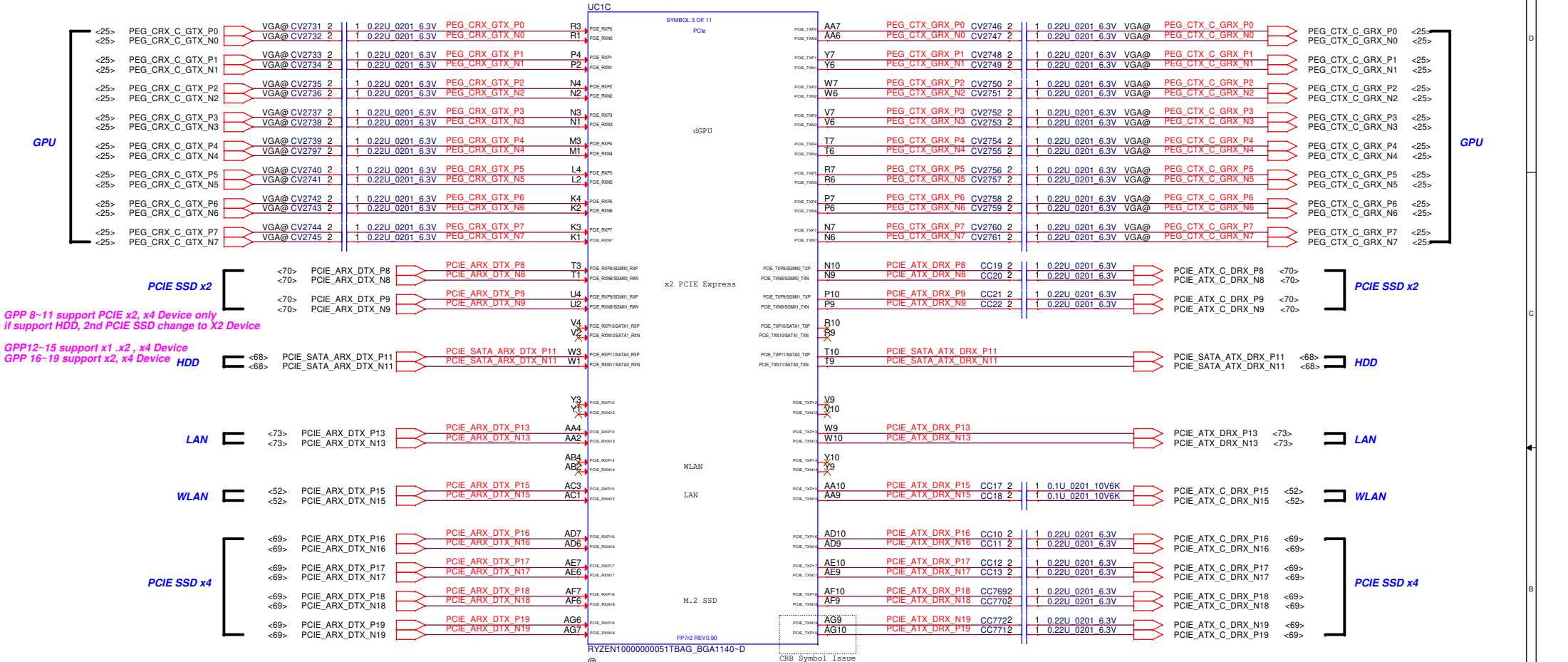
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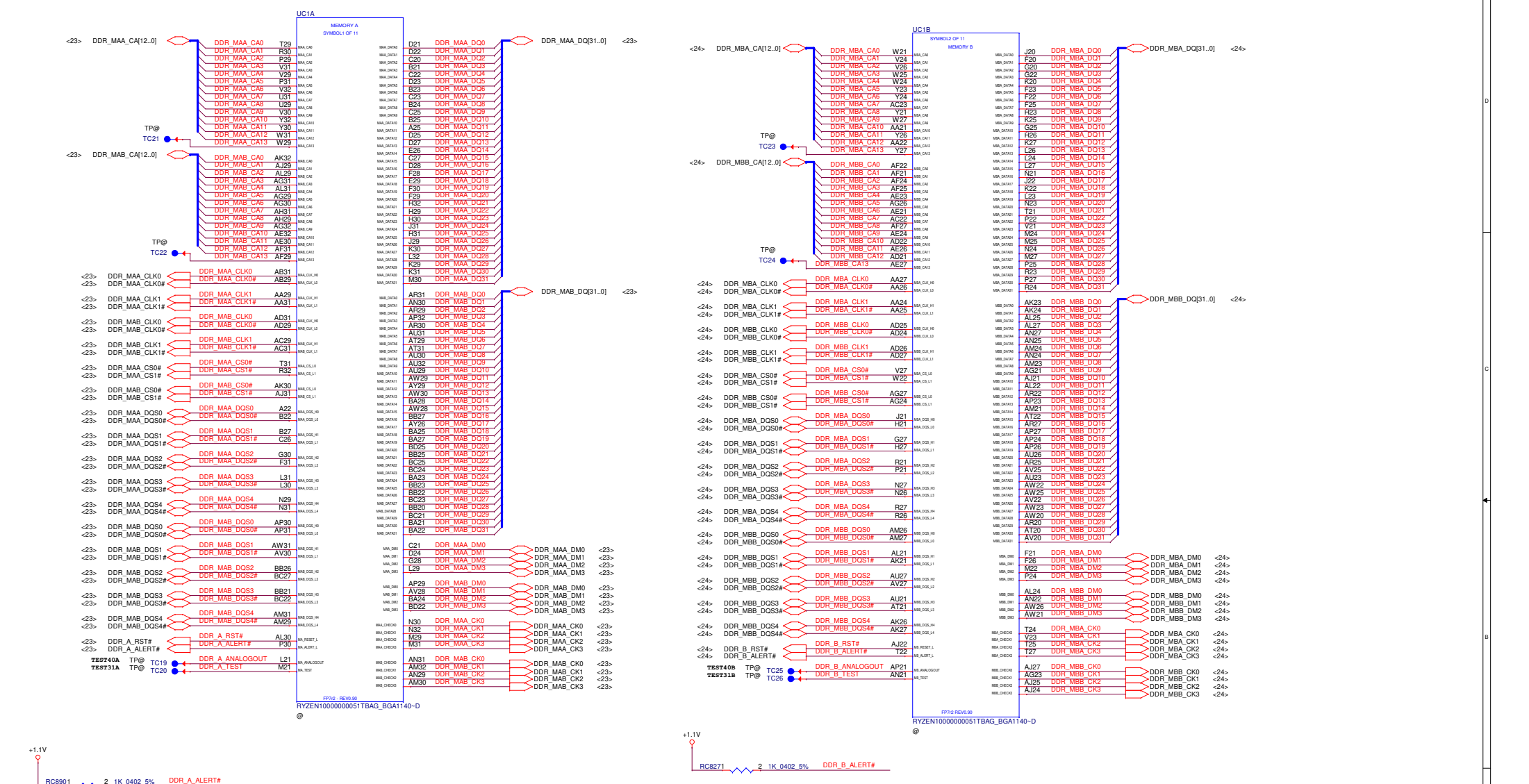
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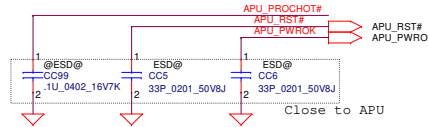
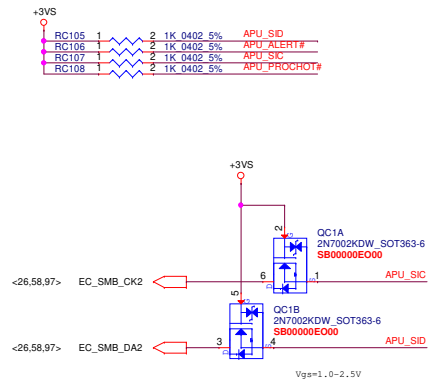
APU PN Table

UC1	ES PN	UC1	PC PN	UC1	PR PN	UC1	IP PN
SA0000ELI00	518@	SA0000F0C00	560@	SA0000F0C10	560PR@	SA0000F0C30	560IP@
S IC RYZEN 100-000000518-41 TBAG BGA 1140 APU S UC1		S IC RYZEN 100-000000560-40 3.1G BGA 1140 APU S UC1		S IC RYZEN 100-000000560 TBA BGA APU S UC1		S IC RYZEN 100-000000560 3.3G APU ABO ! UC1	
SA0000ENT00	532@	SA0000F0A00	561@	SA0000F0A20	561PR@	SA0000F0A60	561IP@
S IC RYZEN 100-000000532-41 TBAG BGA 1140 APU S UC1		S IC RYZEN 100-000000561-40 3G BGA 1140 APU S UC1		S IC RYZEN 100-000000561 TBA BGA APU S UC1		S IC RYZEN 100-000000561 3.2G APU ABO ! UC1	
		SA0000F0B00	562@	SA0000F0B20	562PR@	SA0000F0B60	562IP@
		S IC RYZEN 100-000000562-40 3.2G BGA 1140 APU S UC1		S IC RYZEN 100-000000562 TBA BGA APU S UC1		S IC RYZEN 100-000000562 3.3G APU ABO ! UC1	

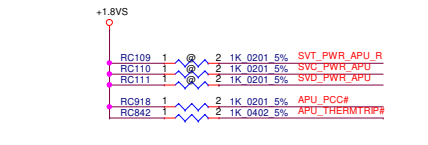
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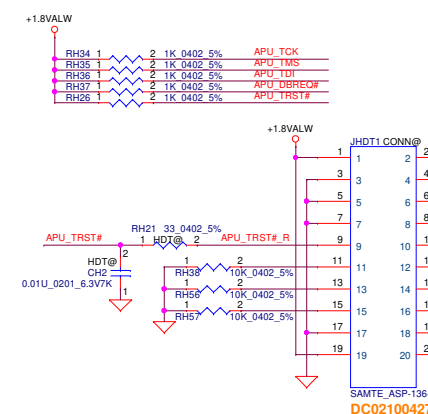
EC/THERM



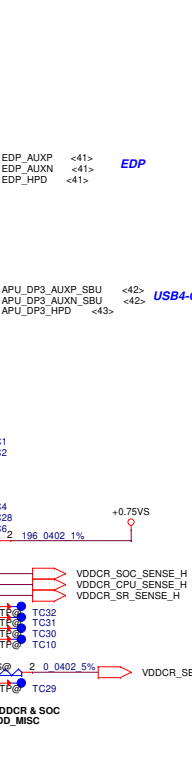
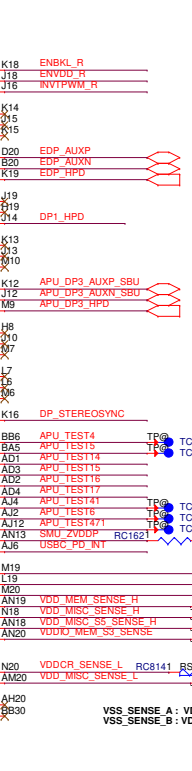
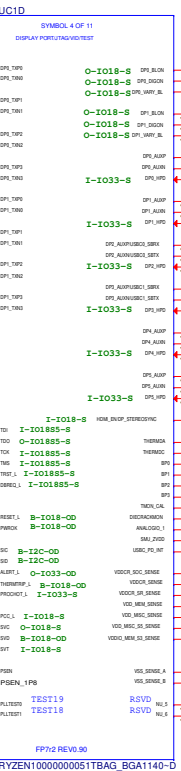
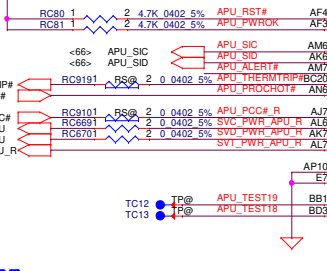
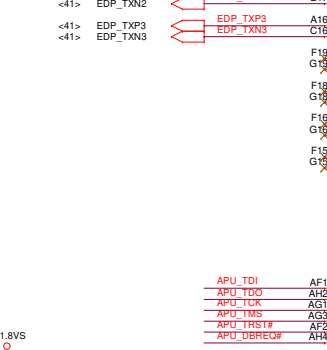
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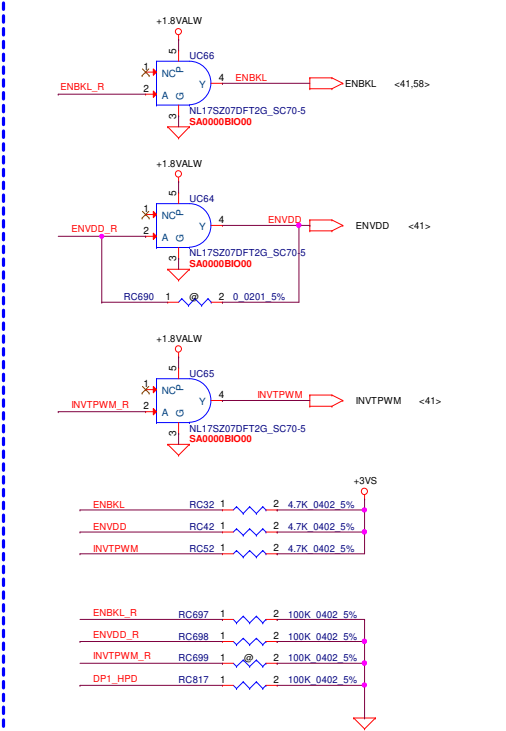
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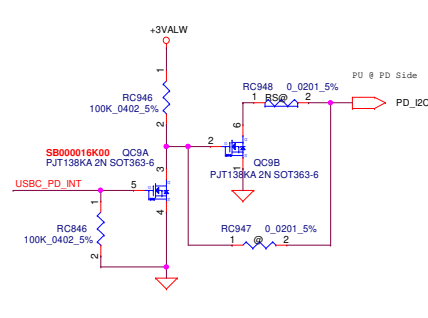
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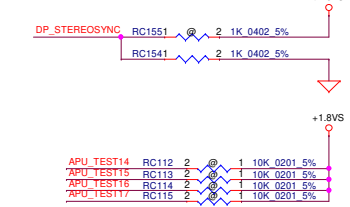
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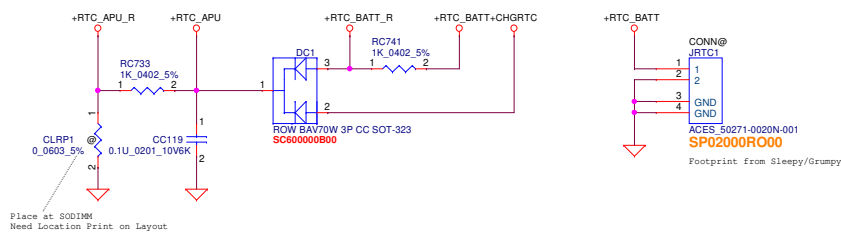
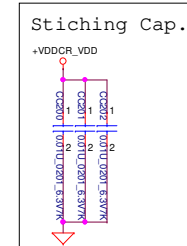
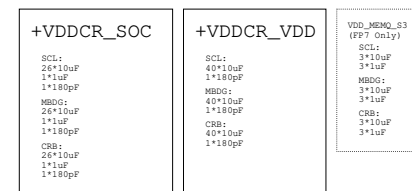
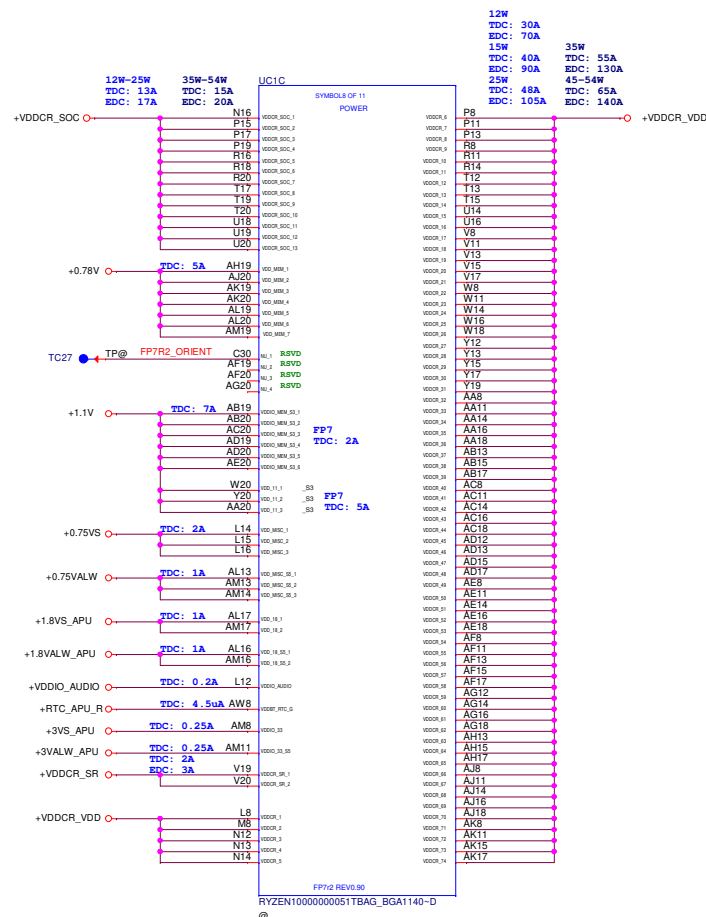
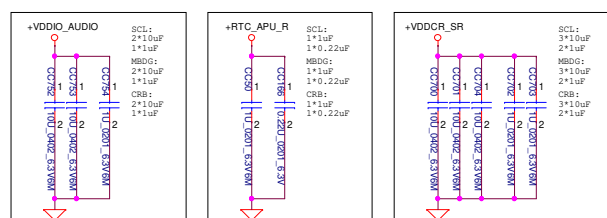
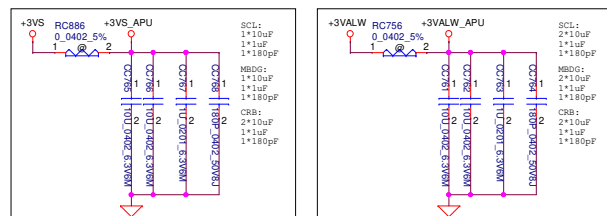
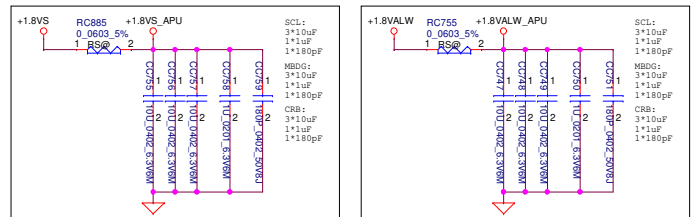
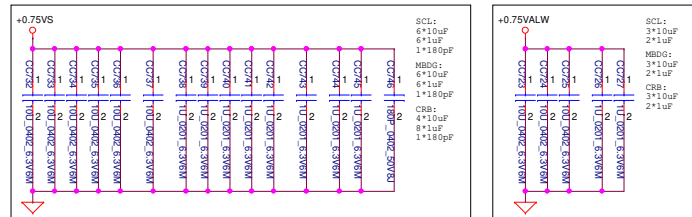
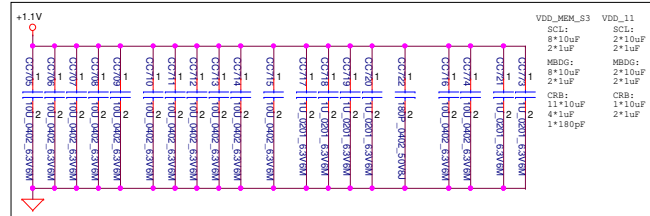
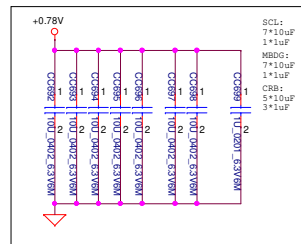


TEST POINT



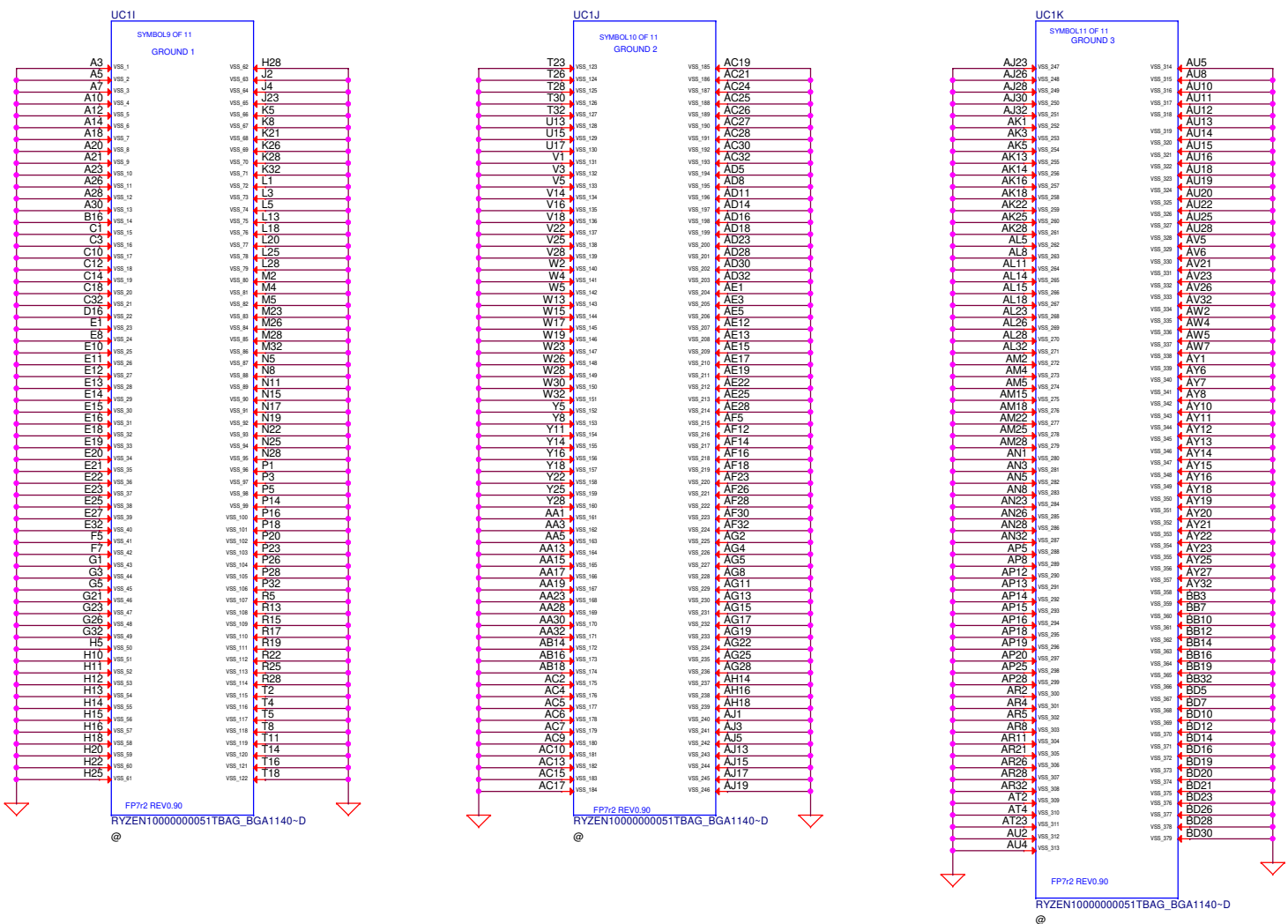
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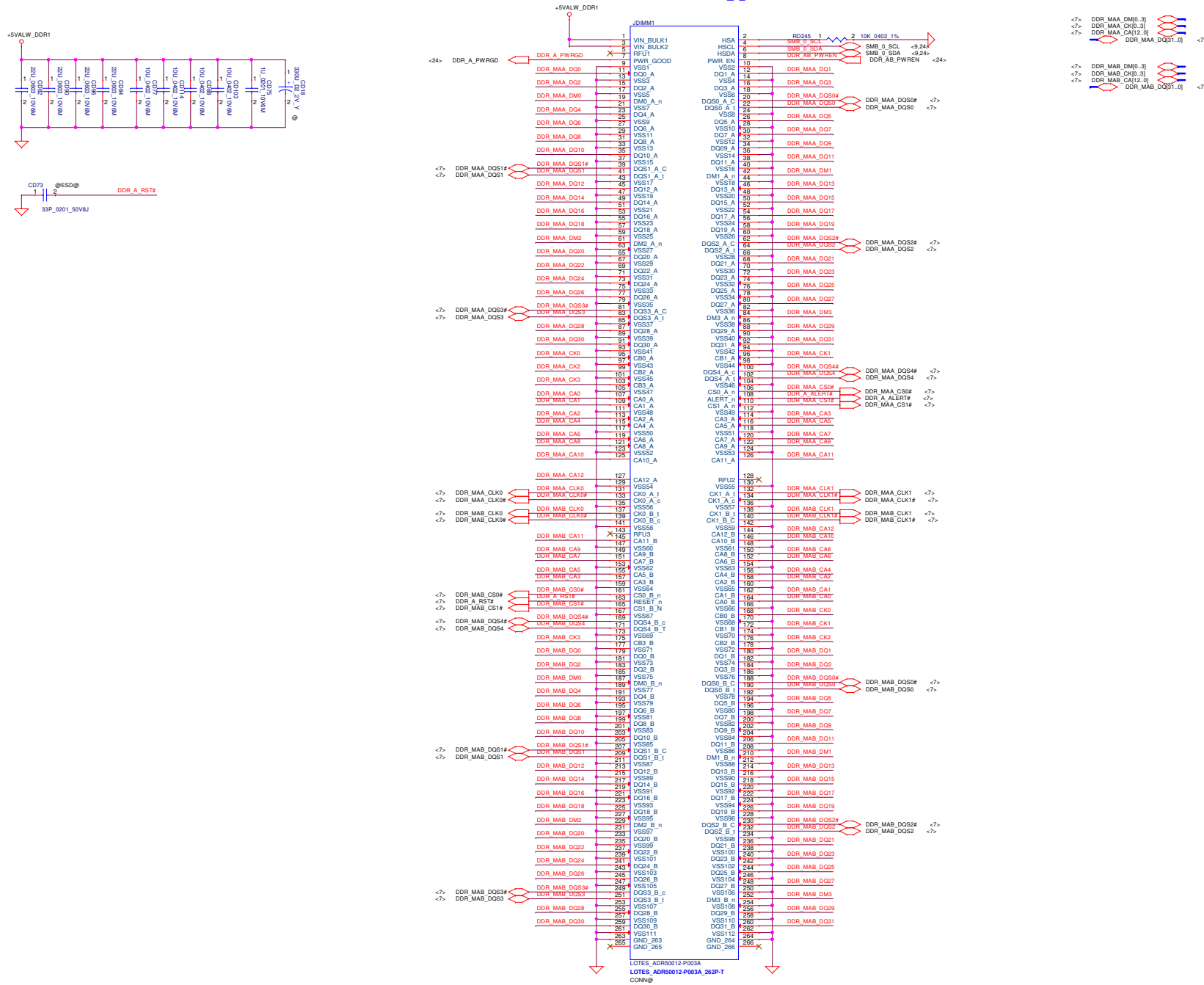
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Reserve

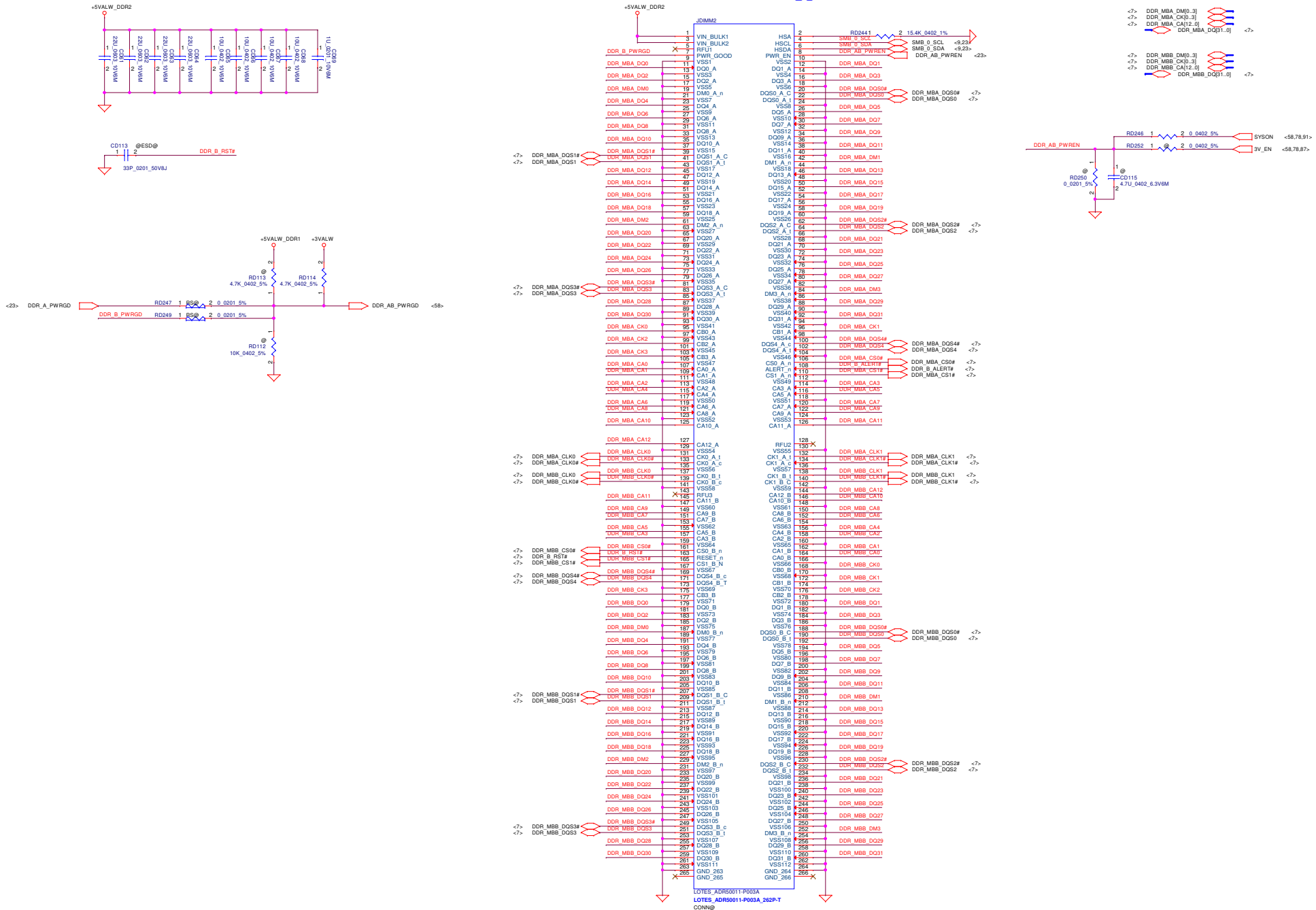
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Reserve Type



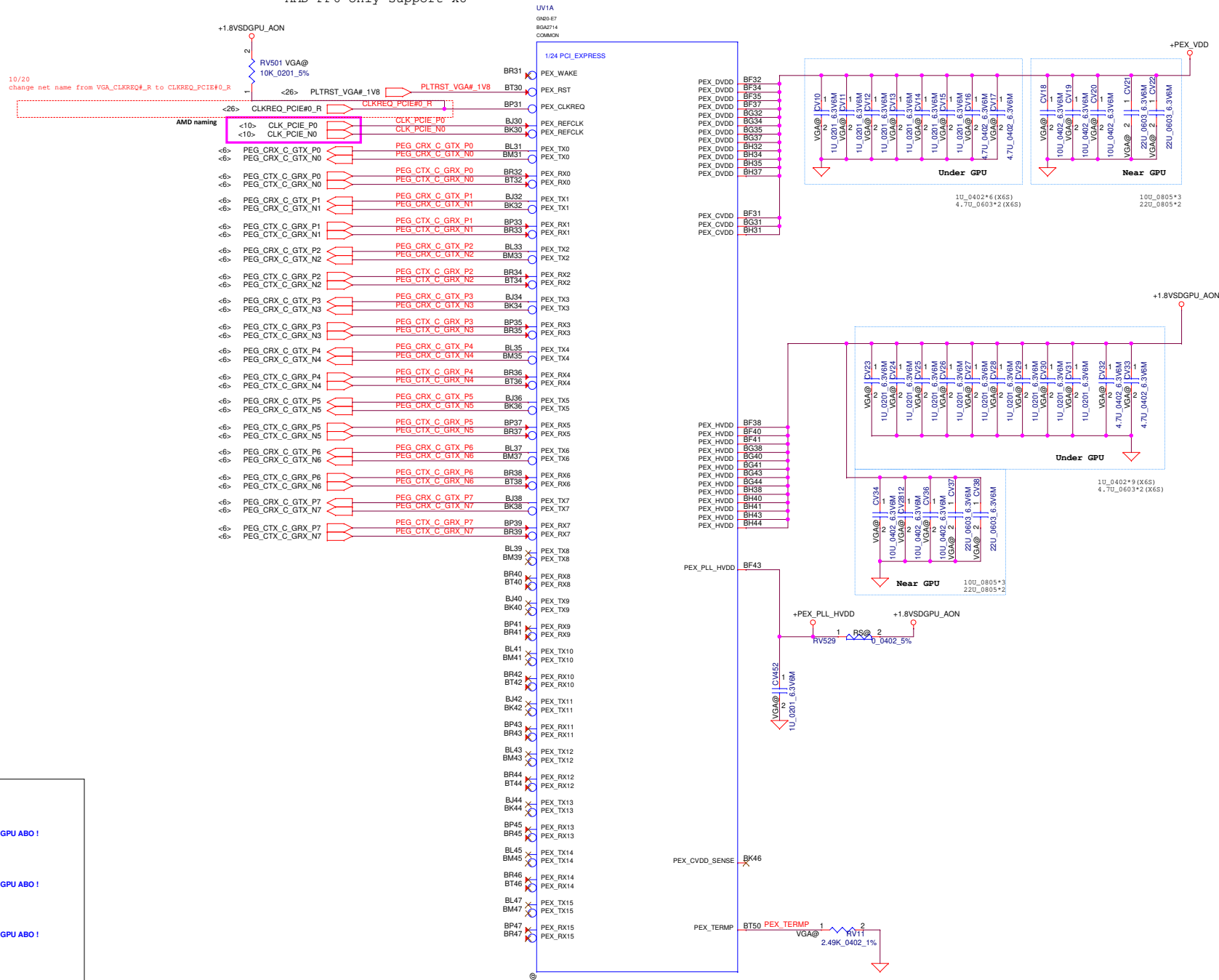
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<p>Doc No: Tuesday, February 22, 2022</p>			Sheet	23 of 122

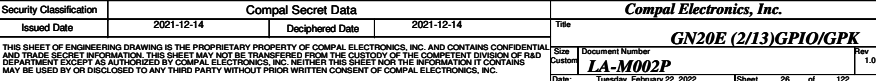
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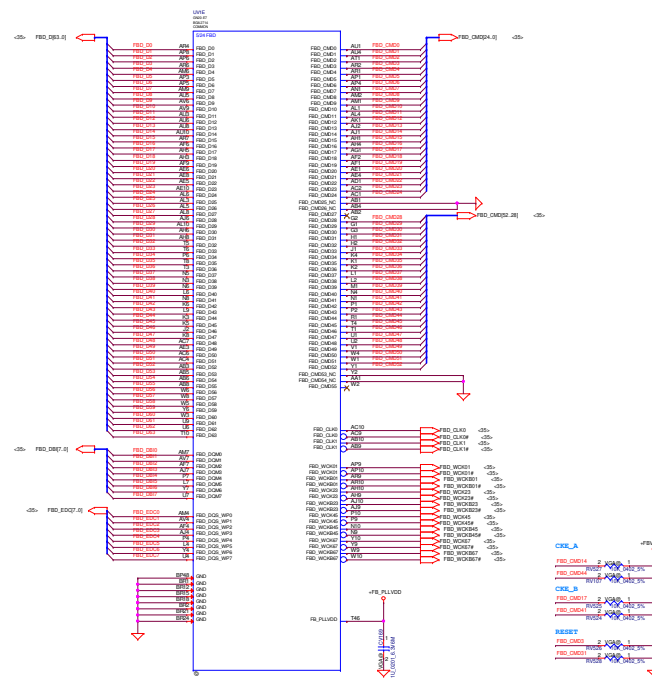
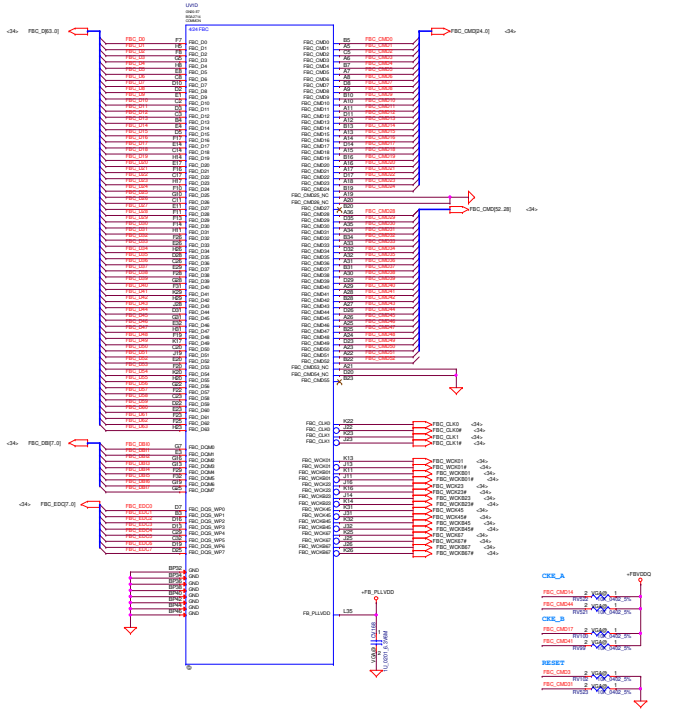
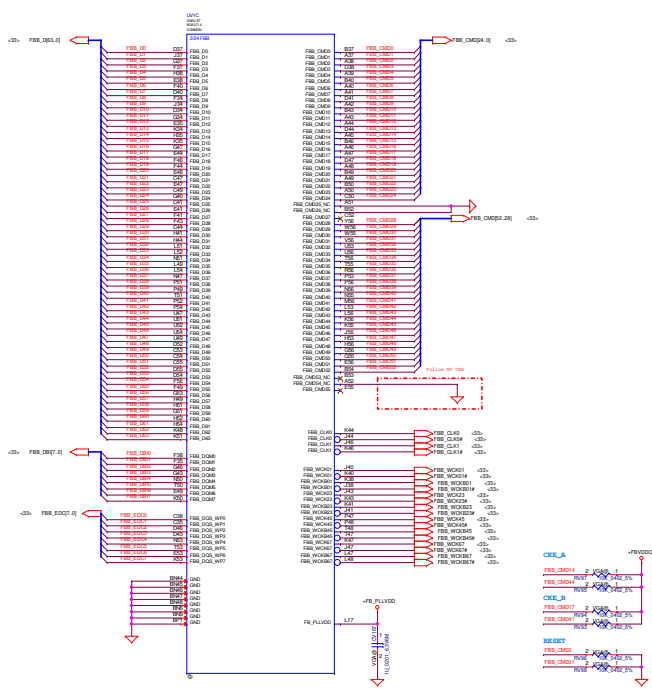
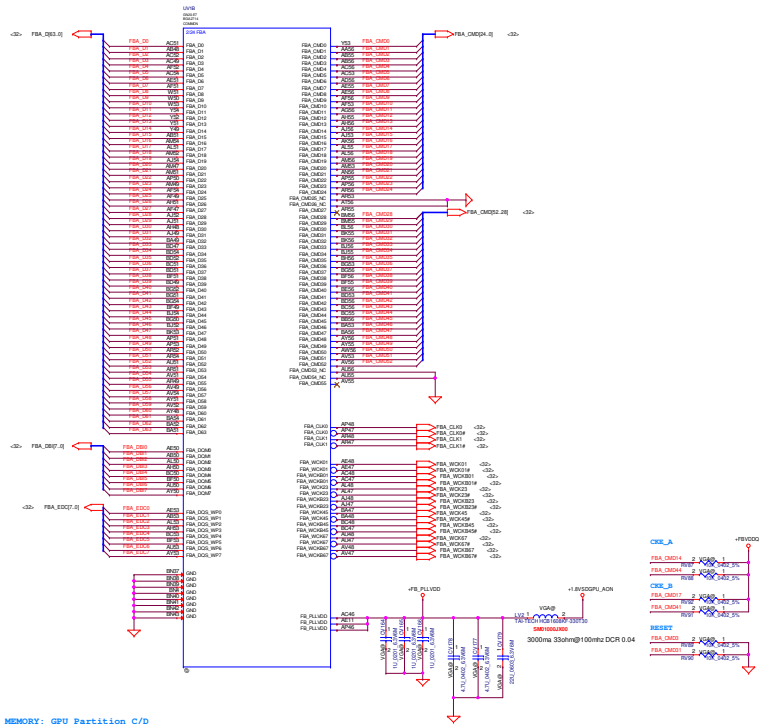


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AMD FP6 only support x8







10/10
SMB_ALT_DDR
0:Single VGA
1:Dual VGA
DEVID_SEL
0:original PCIe ID define
1:re-brand Device ID define
PCIE_CFG
0:normal (full) signal swing
1:reduce signal swing
VGA_DEVICE
0:3D device
1:VGA device

Strap Pins See Note		Functions Selected by This Strapping					
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	0
L	L	H	0	0	0	1	0
L	H	L	0	0	1	0	1
L	H	H	0	1	1	1	1
H	L	L	1	0	0	0	0
H	L	H	1	0	1	0	1
H	H	L	1	1	1	1	1
H	H	H	1	1	1	1	1
L	L	L	1	0	0	0	0
L	L	L	1	0	1	0	1
L	L	H	1	1	1	1	1
L	H	L	1	1	1	1	1
L	H	H	1	1	1	1	1
M	M	M	1	1	1	1	1
M	M	M	1	1	1	1	1
M	M	M	1	1	1	1	1

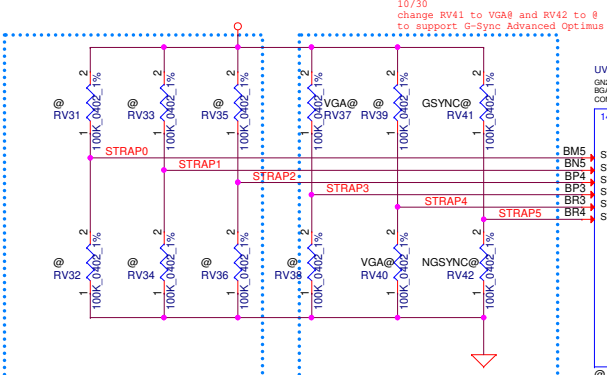
Memory Density	Vendor	Manufacture part Number	Die Revision	Strap	Strap2	Strap1	Strap0	GN20-E7	GN20-E5	GN20-E3	GN20-E1	GN20-E3	GN20-E5
8Gb	Samsung	K4280325BC-HC14	C-die	0x0	L	L	L	V	V (x6)	V (x6)	V	V	V
8Gb	Micron	MT61K256M32JE-14:A	A-die	0x1	L	L	H						
8Gb	Hynix	H56C8H24AIR-S2C	A-die	0x2	L	H	L	V	V (x6)	V (x6)	V	V	V
16Gb	Samsung	K42AF325BM-HC14	M-die	0x9	L	M	L						V

Table 1. GN20-E7 GDDR6 Recommended Memories											
Memory Density	Allowed Memory Configuration	FBVDDQ/V	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Alert	Qual Plan	Status
16Gb	2Chx128Mb/16	1.25V	Samsung	K42AF325BM-HC14	M-die	0x9	14 Gbps	2021	Full	Production candidate	
8Gb	2Chx256Mb/16	1.25V	Samsung	K4280325BC-HC14	C-die	0x0	14 Gbps	2021	Full	Production candidate	

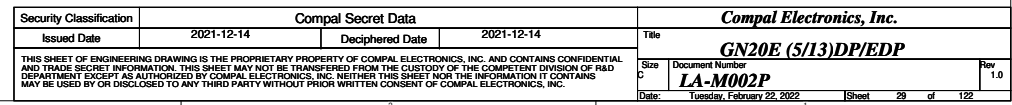
Table 2. GN20-E5 GDDR6 Recommended Memories											
Memory Density	Allowed Memory Configuration	FBVDDQ/V	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Alert	Qual Plan	Status
8Gb	2Chx256Mb/16	1.25V	Samsung	K4280325BC-HC14	C-die	0x0	14 Gbps	2021	Full	Production candidate	
8Gb	2Chx256Mb/16	1.25V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	2021	Full	Production candidate	
8Gb	2Chx256Mb/16	1.25V	Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	2021	Full	Production candidate	

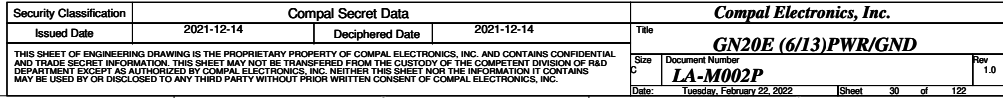
Table 3. GN20-E3 GDDR6 Recommended Memories											
Memory Density	Allowed Memory Configuration	FBVDDQ/V	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Alert	Qual Plan	Status
8Gb	2Chx256Mb/16	1.25V	Samsung	K4280325BC-HC14	C-die	0x0	14 Gbps	2021	Full	Production candidate	
8Gb	2Chx256Mb/16	1.25V	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	2021	Full	Production candidate	
8Gb	2Chx256Mb/16	1.25V	Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	2021	Full	Production candidate	

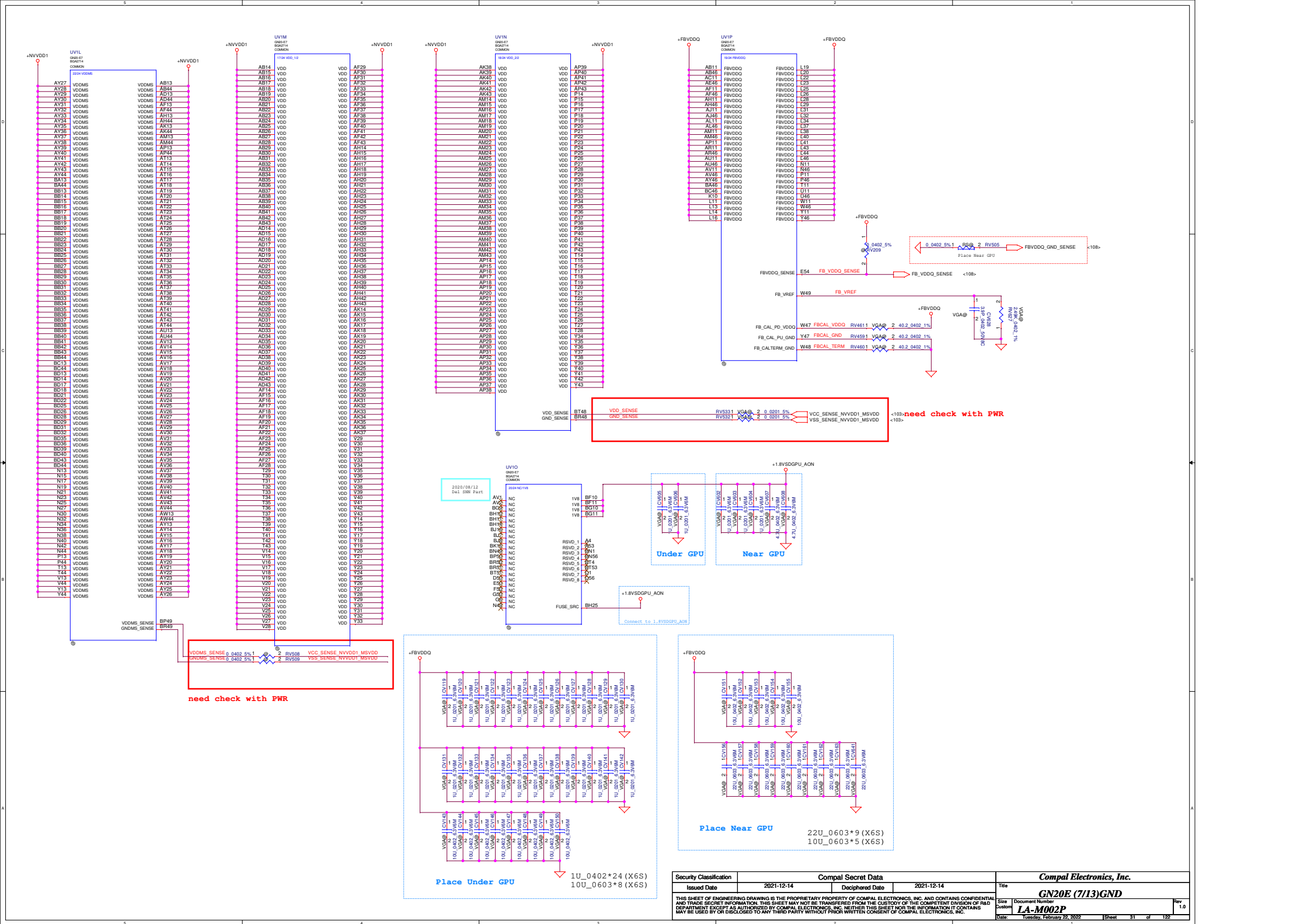
X76VSAM@ UV3	X76VSAM@ UV4	X76VSAM@ UV5	X76VSAM@ UV6	X76VSAM@ UV7	X76VSAM@ UV8
SA0000C6280	SA0000C6280	SA0000C6280	SA0000C6280	SA0000C6280	SA0000C6280
X76VSAM@ UV9	X76VSAM@ UV10				
SA0000C6280	SA0000C6280				
X76VSAM@ RV32	X76VSAM@ RV34	X76VSAM@ RV36			
SD034100380	SD034100380	SD034100380			
100K +1% 0402	100K +1% 0402	100K +1% 0402			
X76VSAM8 - for 6Gb X76VSAM8 + X76VSAM8 - for 8Gb Samsung 8Gb					
X76VHYN@ UV3	X76VHYN@ UV4	X76VHYN@ UV5	X76VHYN@ UV6	X76VHYN@ UV7	X76VHYN@ UV8
SA0000DUW20	SA0000DUW20	SA0000DUW20	SA0000DUW20	SA0000DUW20	SA0000DUW20
X76VHYN@ UV9	X76VHYN@ UV10				
SA0000DUW20	SA0000DUW20				
X76VHYN@ RV32	X76VHYN@ RV33	X76VHYN@ RV36			
SD034100380	SD034100380	SD034100380			
100K +1% 0402	100K +1% 0402	100K +1% 0402			
X76VHYN8 - for 6Gb X76VHYN8 + X76VHYN8 - for 8Gb Hynix 8Gb					
X76V16G@ UV3	X76V16G@ UV4	X76V16G@ UV5	X76V16G@ UV6	X76V16G@ UV7	X76V16G@ UV8
SA0000CBG10	SA0000CBG10	SA0000CBG10	SA0000CBG10	SA0000CBG10	SA0000CBG10
X76V16G@ UV9	X76V16G@ UV10				
SA0000CBG10	SA0000CBG10				
X76V16G@ RV36	X76V16G@ RV32	X76V16G@ RV33	X76V16G@ RV34		
SD034100380	SD034100380	SD034100380	SD034100380		
100K +1% 0402	100K +1% 0402	100K +1% 0402	100K +1% 0402		
X76V16G8 Samsung 16Gb					



HDMI 2.1







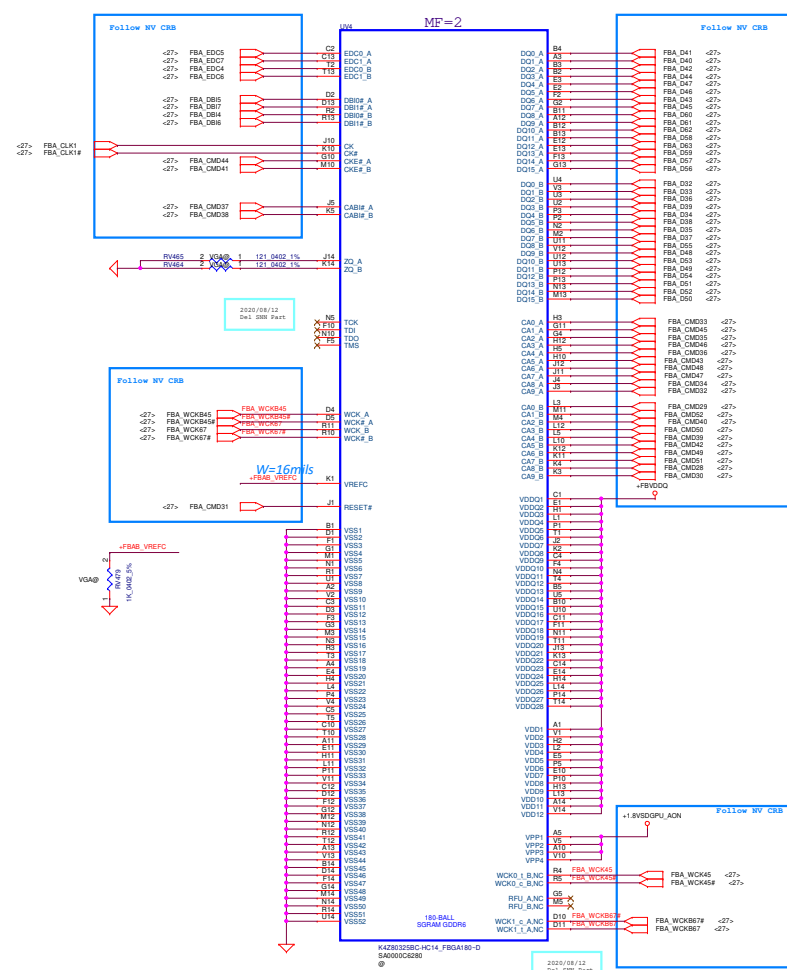
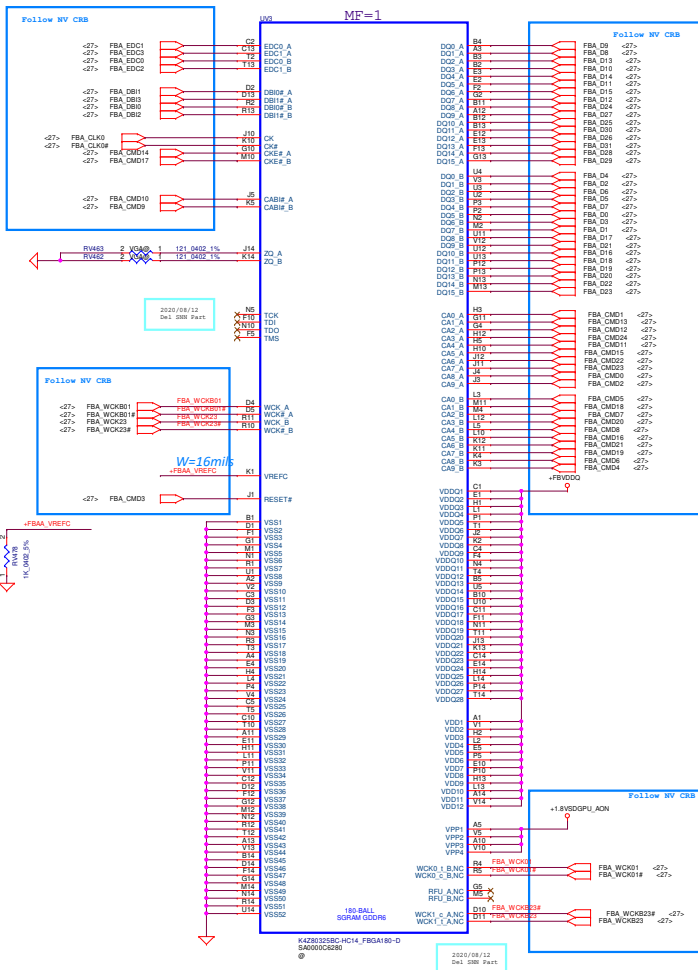


Table 6.4 GDDR6 Mode 3 Mapping, GB5-256

GB5-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 4,5,6,7]	GB5-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBA_CMD0	Bytes 0:1, CA0_A	FBA_CMD28	Bytes 4:5, CA0_B
FBA_CMD1	Bytes 0:1, CA0_A	FBA_CMD29	Bytes 4:5, CA0_B
FBA_CMD2	Bytes 0:1, CA0_A	FBA_CMD30	Bytes 4:5, CA0_B
FBA_CMD3	Bytes 0:1, CA0_A	FBA_CMD31	Bytes 4:5, CA0_B

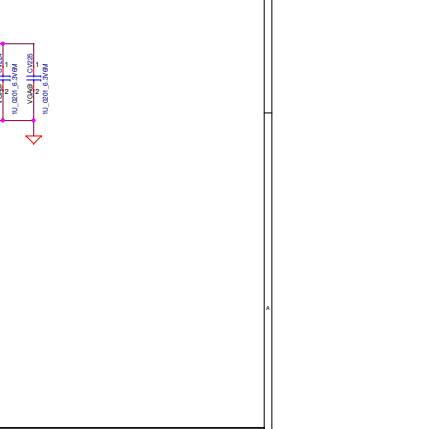
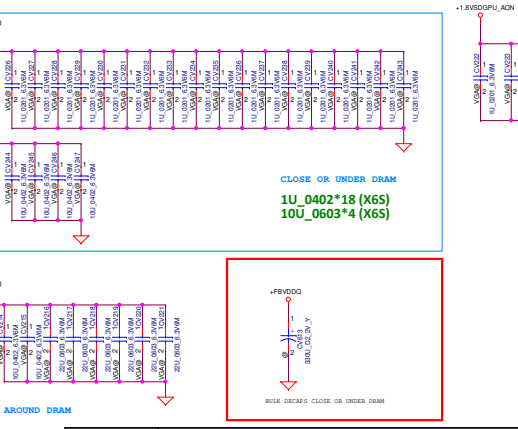
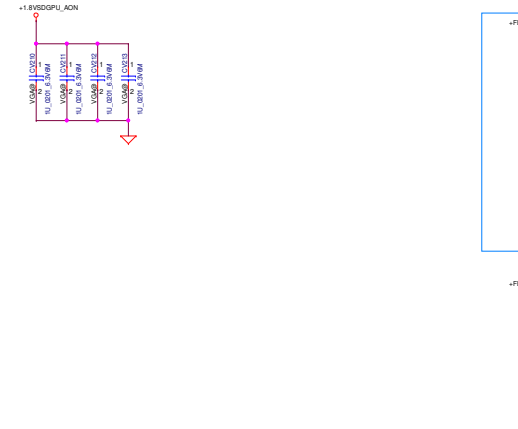
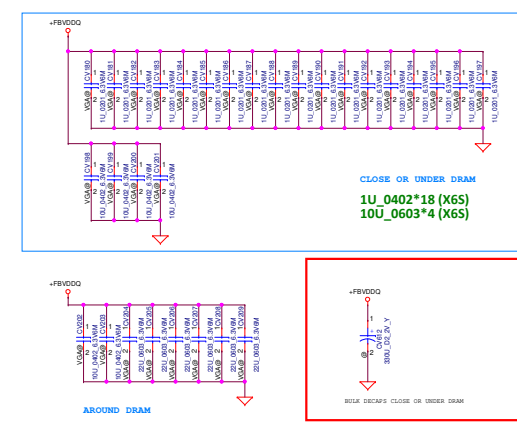
Table 6.4 GDDR6 Mode 3 Mapping, GB5-256 (Continued)

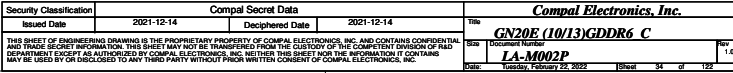
GB5-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 4,5,6,7]	GB5-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBA_CMD4	Bytes 0:1, CA0_A	FBA_CMD32	Bytes 4:5, CA0_B
FBA_CMD5	Bytes 0:1, CA0_A	FBA_CMD33	Bytes 4:5, CA0_B
FBA_CMD6	Bytes 0:1, CA0_A	FBA_CMD34	Bytes 4:5, CA0_B
FBA_CMD7	Bytes 0:1, CA0_A	FBA_CMD35	Bytes 4:5, CA0_B
FBA_CMD8	Bytes 0:1, CA0_A	FBA_CMD36	Bytes 4:5, CA0_B
FBA_CMD9	Bytes 0:1, CA0_A	FBA_CMD37	Bytes 4:5, CA0_B
FBA_CMD10	Bytes 0:1, CA0_A	FBA_CMD38	Bytes 4:5, CA0_B
FBA_CMD11	Bytes 0:1, CA0_A	FBA_CMD39	Bytes 4:5, CA0_B
FBA_CMD12	Bytes 0:1, CA0_A	FBA_CMD40	Bytes 4:5, CA0_B
FBA_CMD13	Bytes 0:1, CA0_A	FBA_CMD41	Bytes 4:5, CA0_B
FBA_CMD14	Bytes 0:1, CA0_A	FBA_CMD42	Bytes 4:5, CA0_B
FBA_CMD15	Bytes 0:1, CA0_A	FBA_CMD43	Bytes 4:5, CA0_B
FBA_CMD16	Bytes 0:1, CA0_A	FBA_CMD44	Bytes 4:5, CA0_B
FBA_CMD17	Bytes 0:1, CA0_A	FBA_CMD45	Bytes 4:5, CA0_B
FBA_CMD18	Bytes 0:1, CA0_A	FBA_CMD46	Bytes 4:5, CA0_B
FBA_CMD19	Bytes 0:1, CA0_A	FBA_CMD47	Bytes 4:5, CA0_B
FBA_CMD20	Bytes 0:1, CA0_A	FBA_CMD48	Bytes 4:5, CA0_B
FBA_CMD21	Bytes 0:1, CA0_A	FBA_CMD49	Bytes 4:5, CA0_B

Table 6.4 GDDR6 Mode 3 Mapping, GB5-256 (Continued)

GB5-256	GPU FB Channel 0 (Data Bits [31:0]) [Bytes 4,5,6,7]	GB5-256	GPU FB Channel 1 (Data Bits [63:32]) [Bytes 4,5,6,7]
FBA_CMD22	Bytes 0:1, CA0_A	FBA_CMD50	Bytes 4:5, CA0_B
FBA_CMD23	Bytes 0:1, CA0_A	FBA_CMD51	Bytes 4:5, CA0_B
FBA_CMD24	Bytes 0:1, CA0_A	FBA_CMD52	Bytes 4:5, CA0_B
FBA_CMD25	Bytes 0:1, CA0_A	FBA_CMD53	Bytes 4:5, CA0_B
FBA_CMD26	Bytes 0:1, CA0_A	FBA_CMD54	Bytes 4:5, CA0_B
FBA_CMD27	Bytes 0:1, CA0_A	FBA_CMD55	Bytes 4:5, CA0_B
FBA_CMD28	Bytes 0:1, CA0_A	FBA_CMD56	Bytes 4:5, CA0_B
FBA_CMD29	Bytes 0:1, CA0_A	FBA_CMD57	Bytes 4:5, CA0_B
FBA_CMD30	Bytes 0:1, CA0_A	FBA_CMD58	Bytes 4:5, CA0_B
FBA_CMD31	Bytes 0:1, CA0_A	FBA_CMD59	Bytes 4:5, CA0_B

Note:
1. GPU debug pins, not connected to DRAM.
2. Bytes 6,7 correspond to DRAM Channel A, Bytes 7,8 correspond to DRAM Channel B.
3. Bytes 4,5 correspond to DRAM Channel A, Bytes 6,7 correspond to DRAM Channel B.





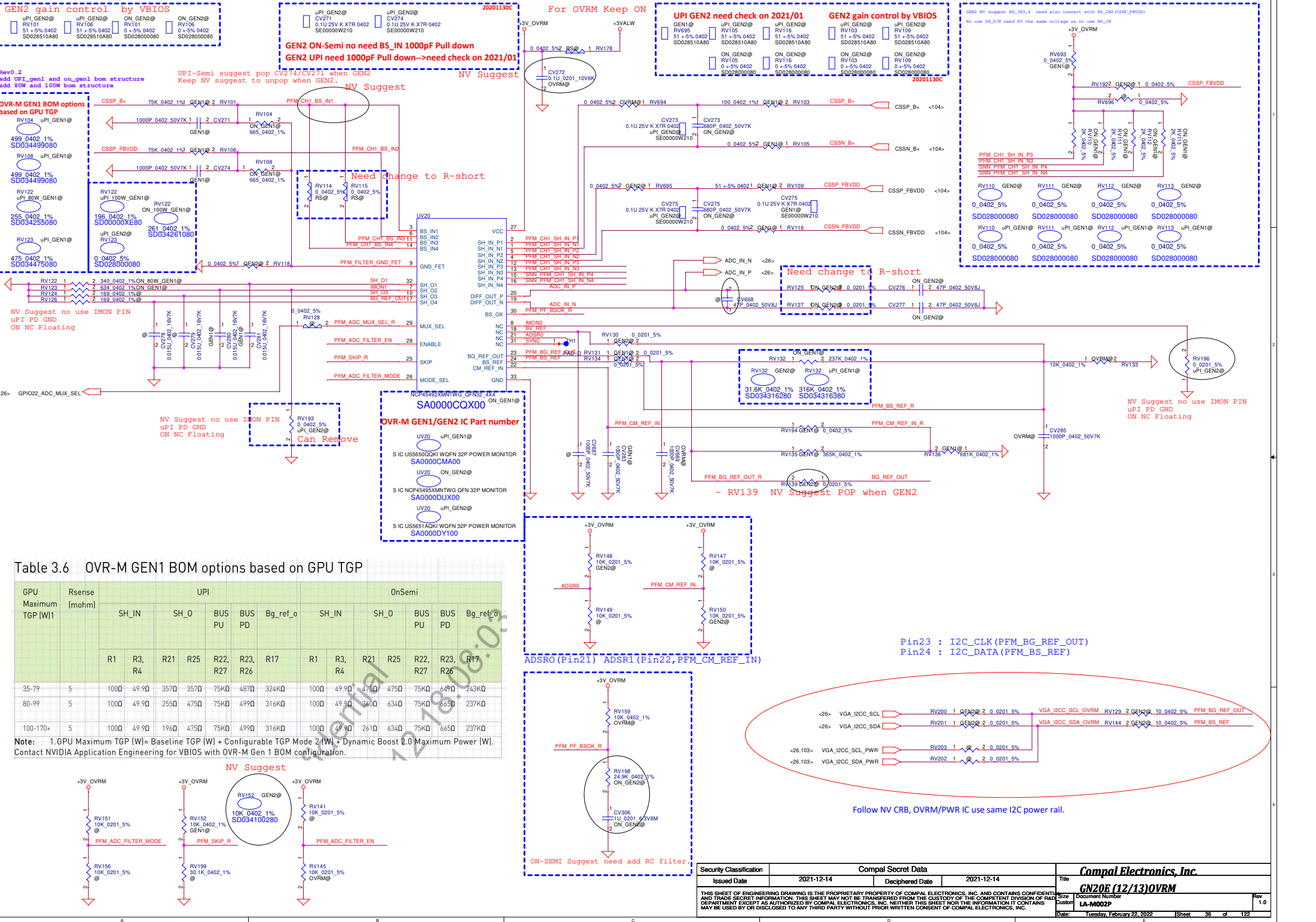
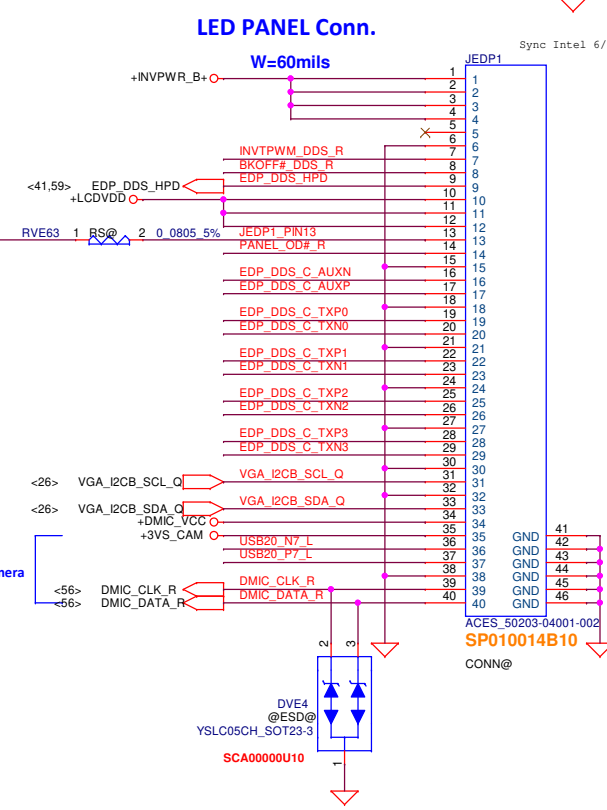
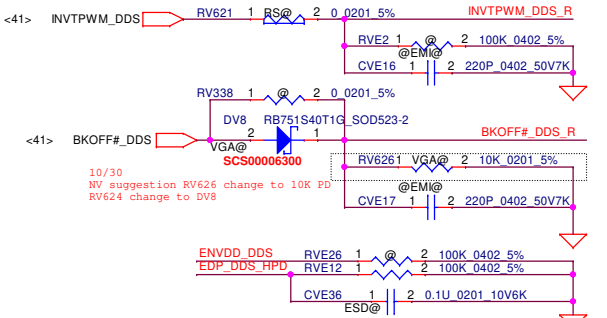
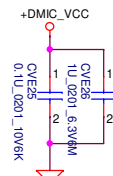
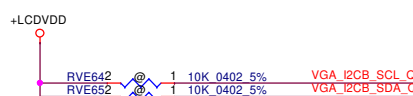
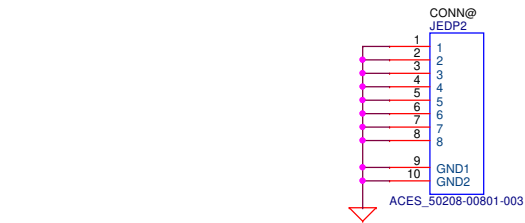
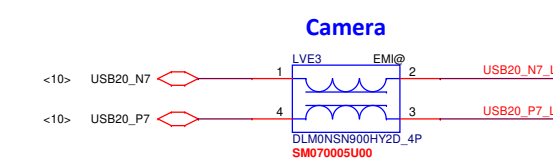
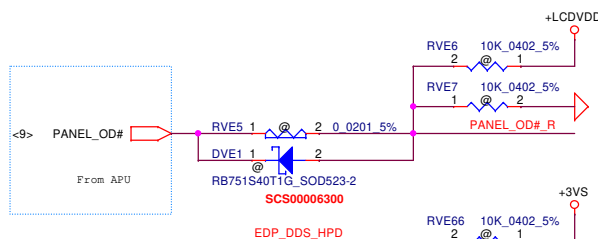
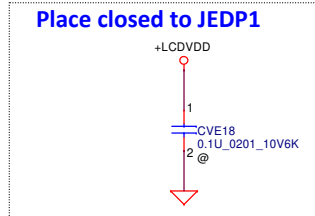
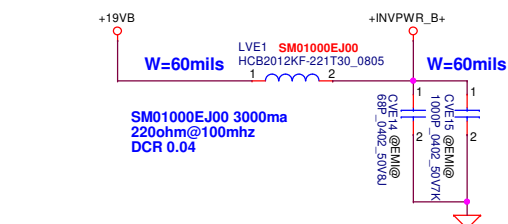
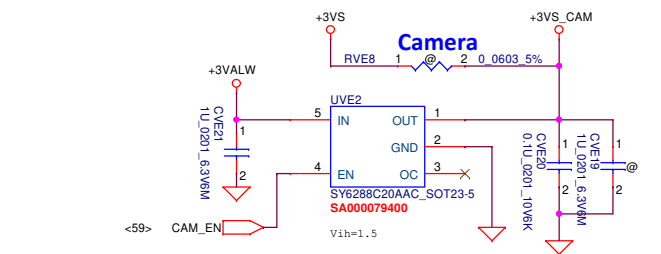
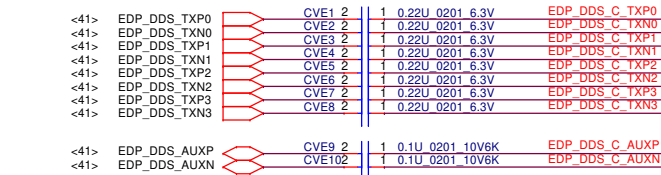
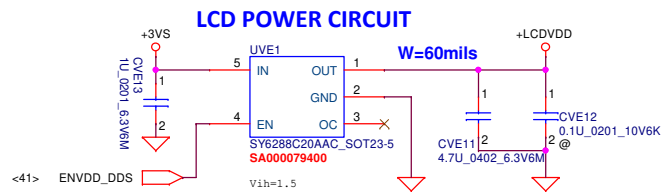


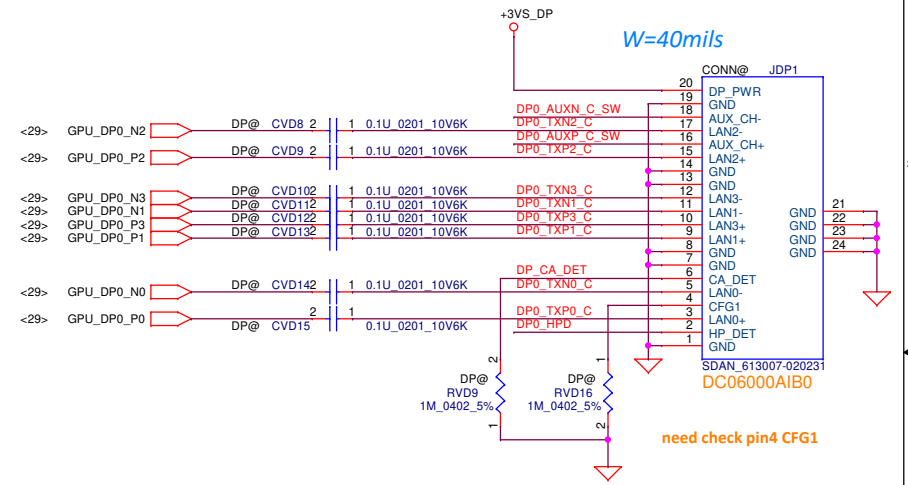
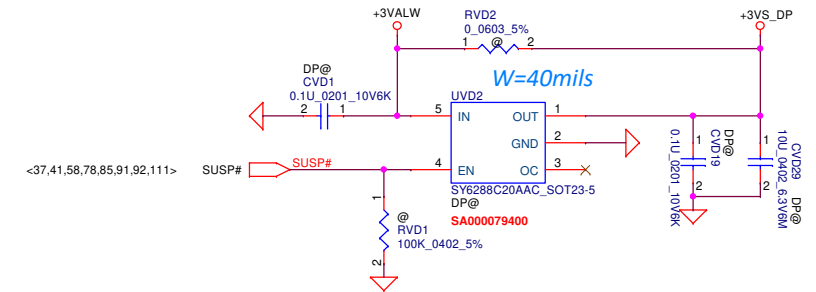
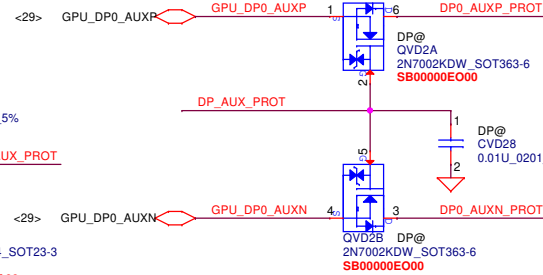
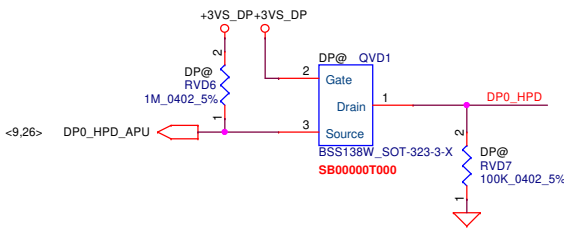
Table 3.6 OVR-M GEN1 BOM options based on GPU TGP

GPU Maximum TGP (W)	Rsense (mohm)	UPI							OnSemi						
		SH_IN		SH_O		BUS PU	BUS PD	Bg_ref_o	SH_IN		SH_O		BUS PU	BUS PD	Bg_ref_o
		R1	R3, R4	R21	R25	R22, R27	R23, R26	R17	R1	R3, R4	R21	R25	R22, R27	R23, R26	R17
35-79	5	1000	49.9K	357K	357K	75K	487K	324K	1000	49.9K	475K	475K	75K	649K	243K
80-99	5	1000	49.9K	255K	475K	75K	499K	316K	1000	49.9K	340K	634K	75K	665K	237K
100-170+	5	100K	49.9K	196K	475K	75K	499K	316K	1000	49.9K	261K	634K	75K	665K	237K

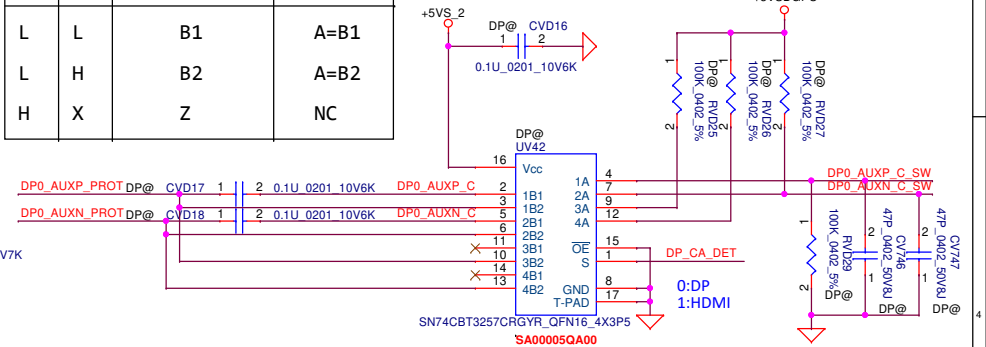
Note: 1. GPU Maximum TGP (W)= Baseline TGP (W) + Configurable TGP Mode 2 (W) + Dynamic Boost 2.0 Maximum Power (W).
Contact NVIDIA Application Engineering for VBIOS with OVR-M Gen 1 BOM configuration.



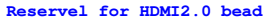
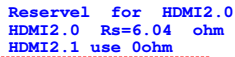
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OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC



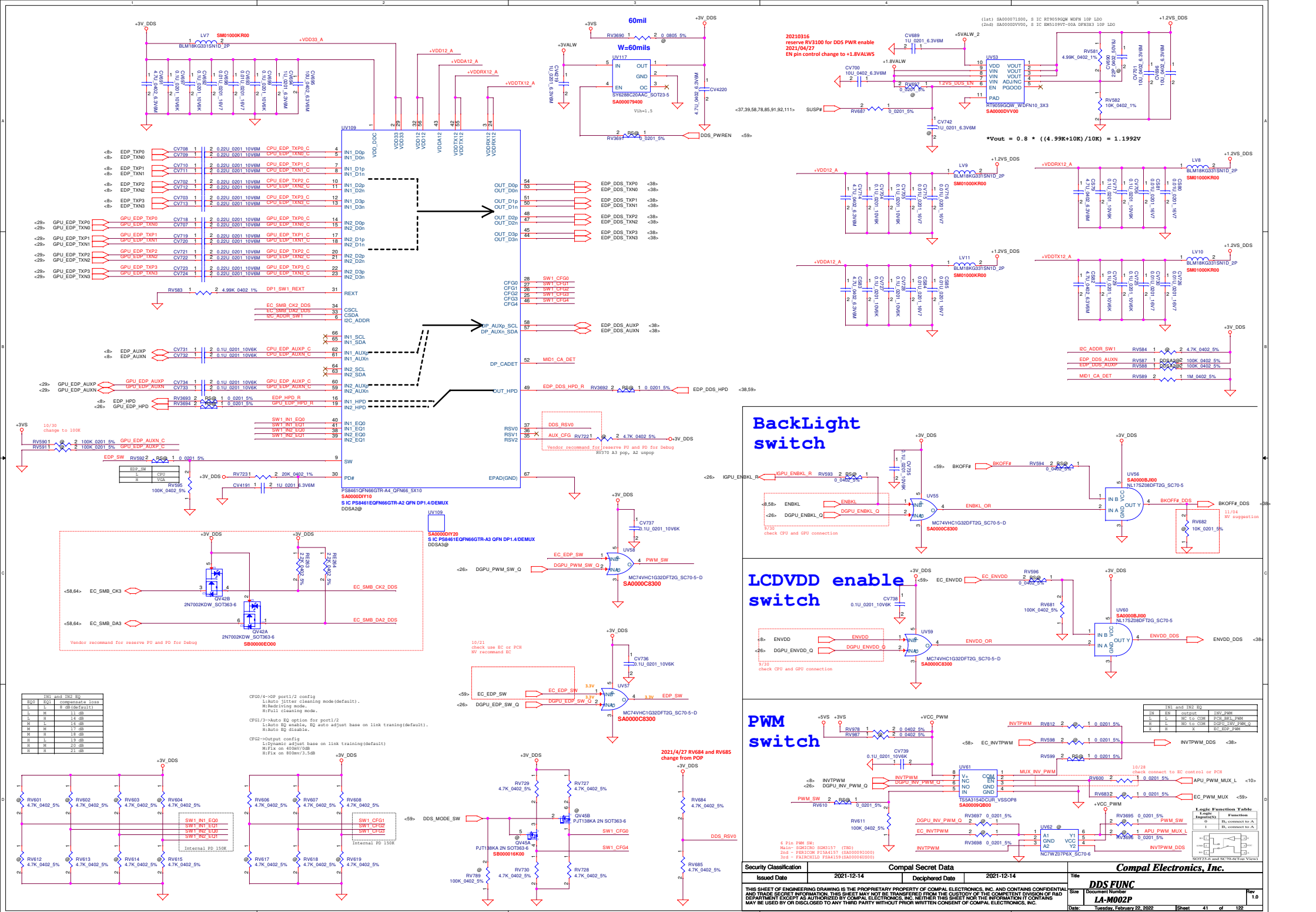
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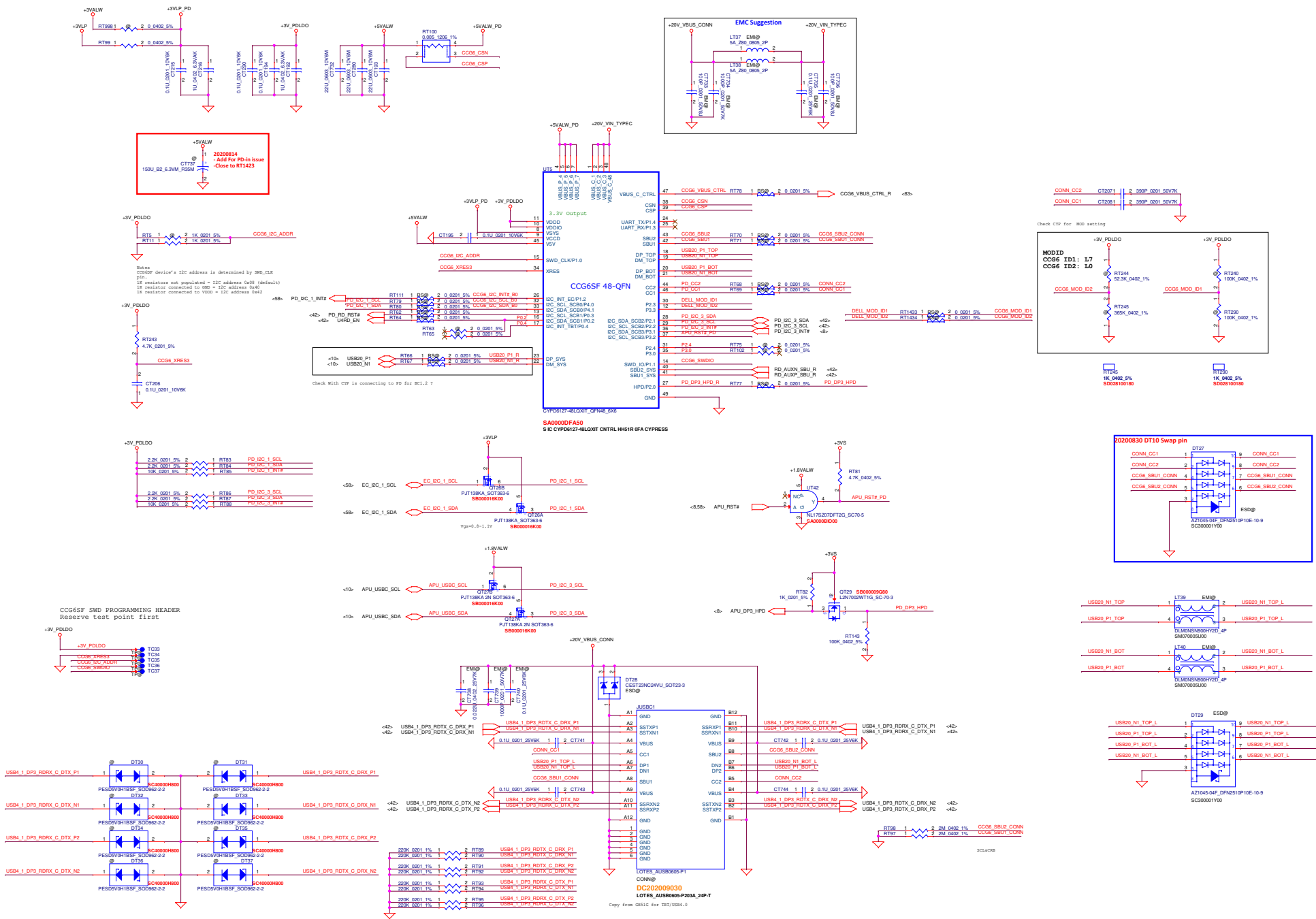
**Compal Electronics, Inc.****HDMI CONN**

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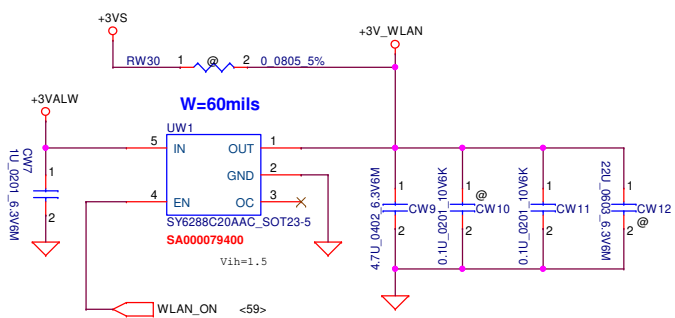
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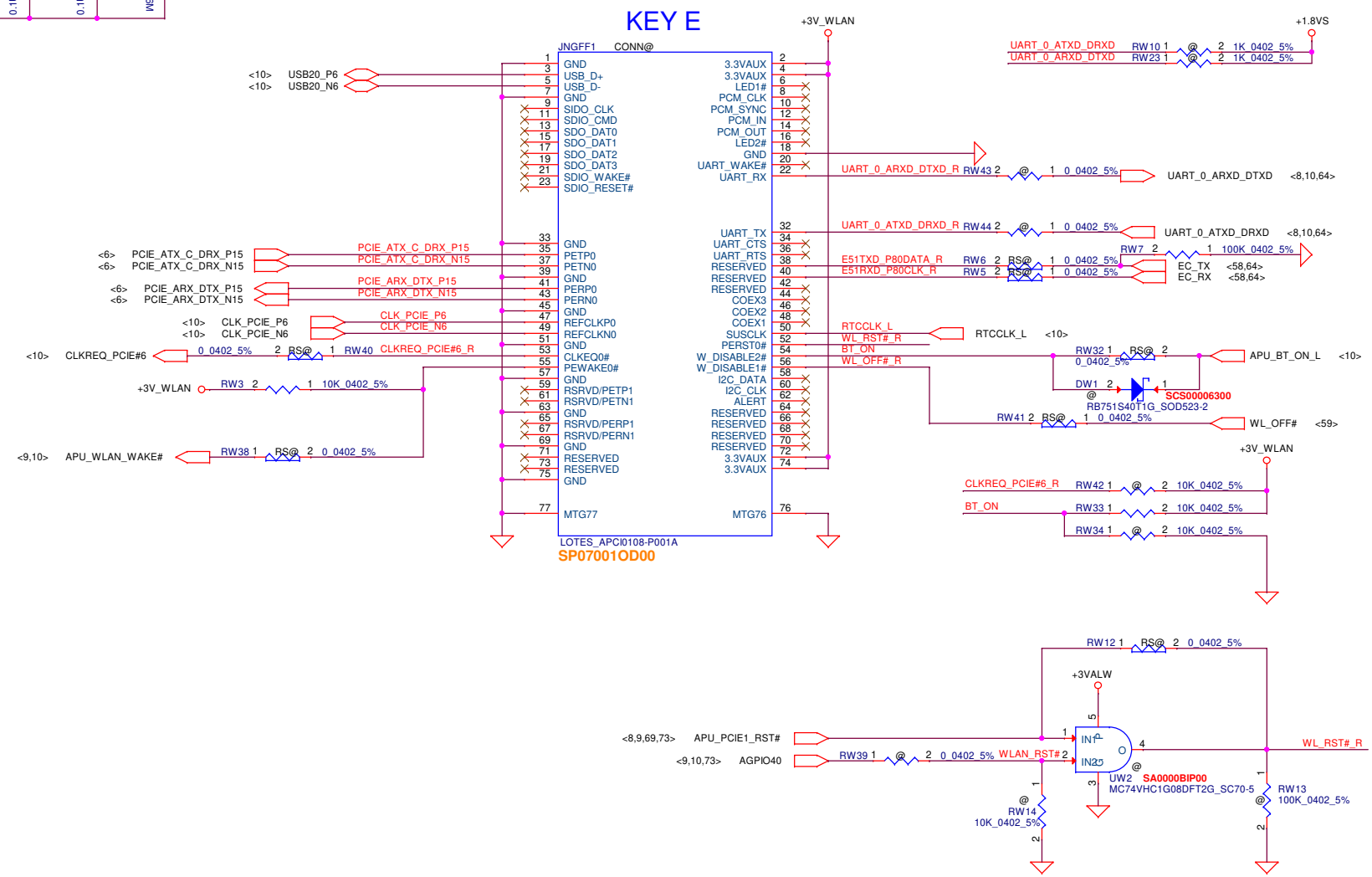
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Wireless LAN



NGFF WL+BT (KEY E)

74	1.1V	GND	75
72	1.1V	RESERVED/REFCLKN1	73
70	UM_Power_SRC(GPIO)/PEWake#	RESERVED/REFCLKP1	71
68	UM_Power_SINK/CLKREQ#	GND	69
66	Reserved/PERn1	Reserved/PERn1	67
64	Reserved/PERP1	Reserved/PERP1	65
62	RESERVED	GND	63
60	ALERT# (I/O/3.3)	Reserved/PETn1	61
58	IQC CLK (I/O/3.3)	Reserved/PETp1	59
56	IQC DATA (I/O/3.3)	GND	57
54	W_DISABLE#1 (O/I/3.3V)	PEWake# (O/I/3.3V)	55
52	Reserved/W_DISABLE#2 (O/I/3.3V)	CLKREQ# (O/I/3.3V)	53
50	PERST# (O/I/3.3V)	GND	51
48	SUSCLK(30kHz) (O/I/3.3V)	REFCLKN0	49
46	COEX1 (I/O/1.8V)	REFCLKP0	47
44	COEX2 (O/I/1.8V)	GND	45
42	COEX3 (O/I/1.8V)	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	VENDOR DEFINED	PETn0	37
34	UART RTS (O/I/1.8V)	PETp0	35
32	UART CTS (I/O/1.8V)	GND	33
30	UART Tx (O/I/1.8V)	GND	31
28	UART Rx (I/O/1.8V)	GND	29
26	UART Wake# (I/O/3.3V)	GND	27
24	SDIO Wake# (I/O/1.8V)	GND	25
22	SDIO DAT0 (O/I/1.8V)	GND	23
20	SDIO DAT1 (O/I/1.8V)	GND	21
18	SDIO DAT2 (O/I/1.8V)	GND	19
16	SDIO DAT3 (O/I/1.8V)	GND	17
14	SDIO DAT0 (O/I/1.8V)	GND	15
12	SDIO DAT1 (O/I/1.8V)	GND	13
10	SDIO DAT2 (O/I/1.8V)	GND	11
8	SDIO DAT3 (O/I/1.8V)	GND	9
6	SDIO CLK (O/I/1.8V)	GND	7
4	SDIO CMD (O/I/1.8V)	GND	5
2	SDIO CMD (O/I/1.8V)	GND	3



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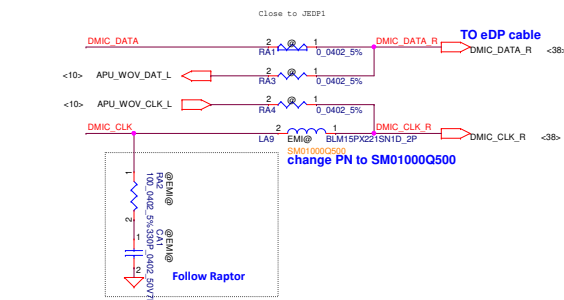
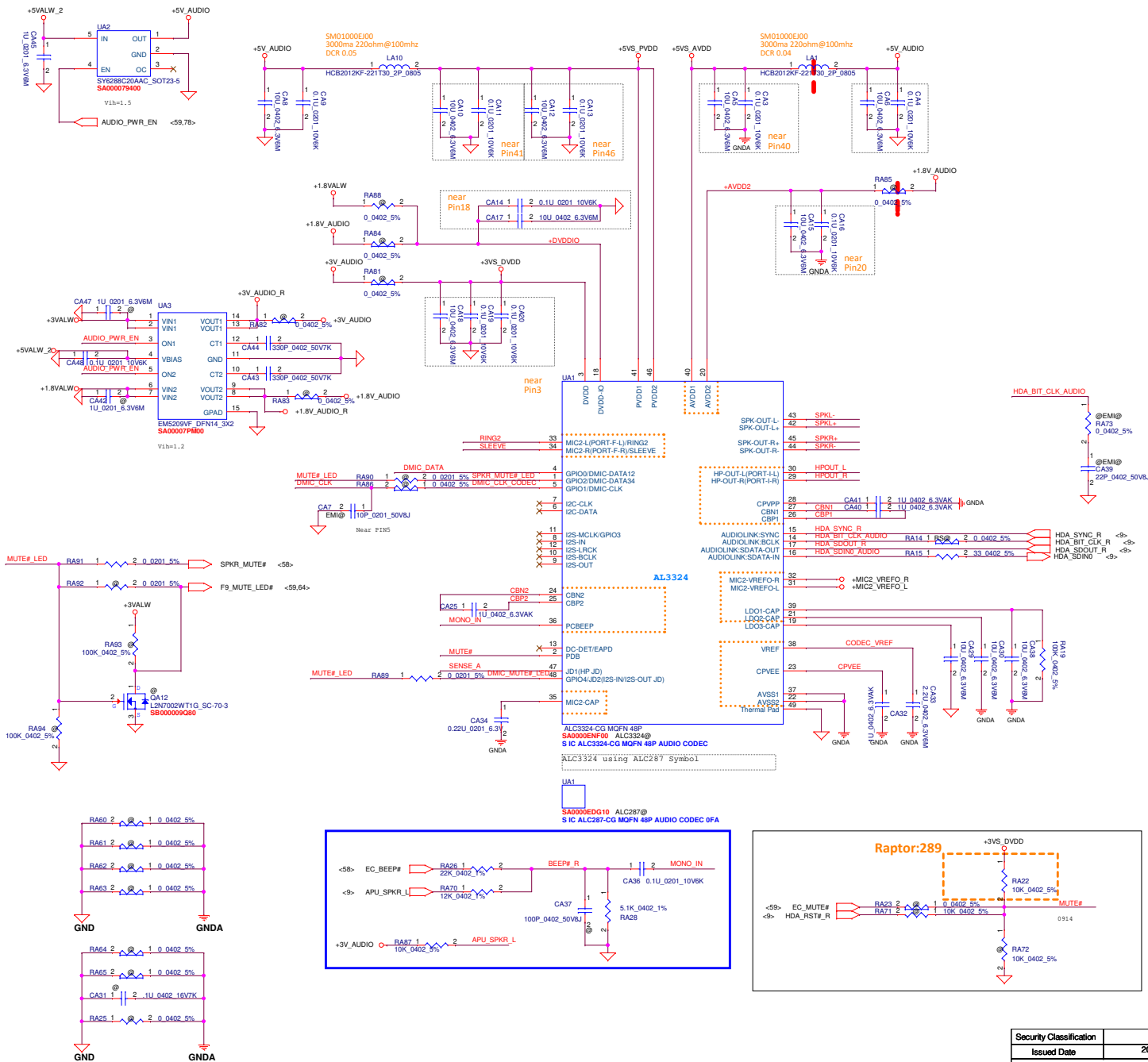
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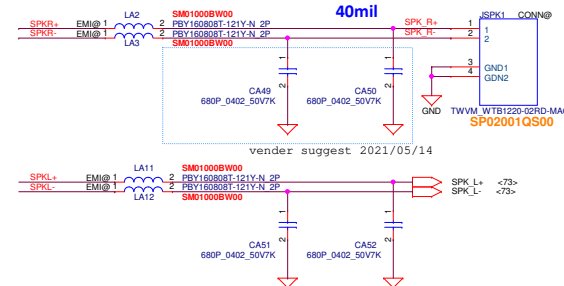
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HD Audio Codec



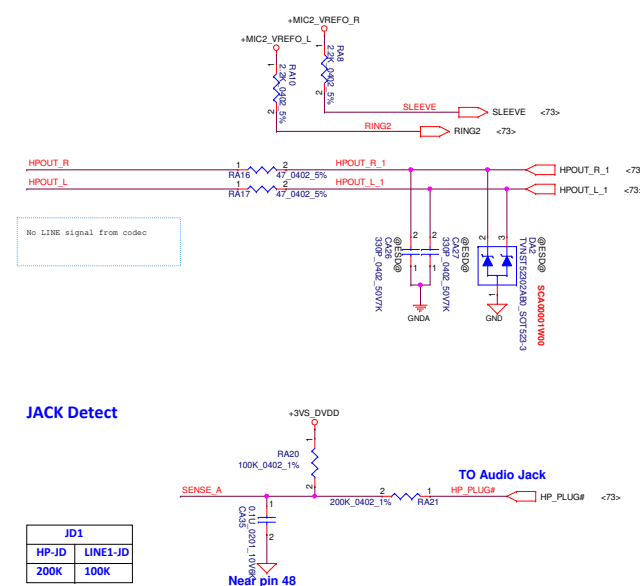
Int. Speaker Conn.



Reserve for EMI

Headphone Out

EMI request for solve EMI noise: SM010000W00



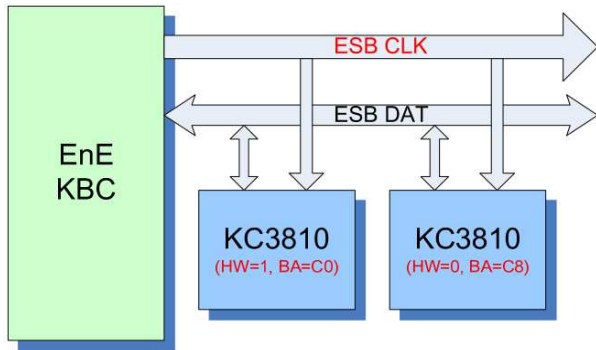
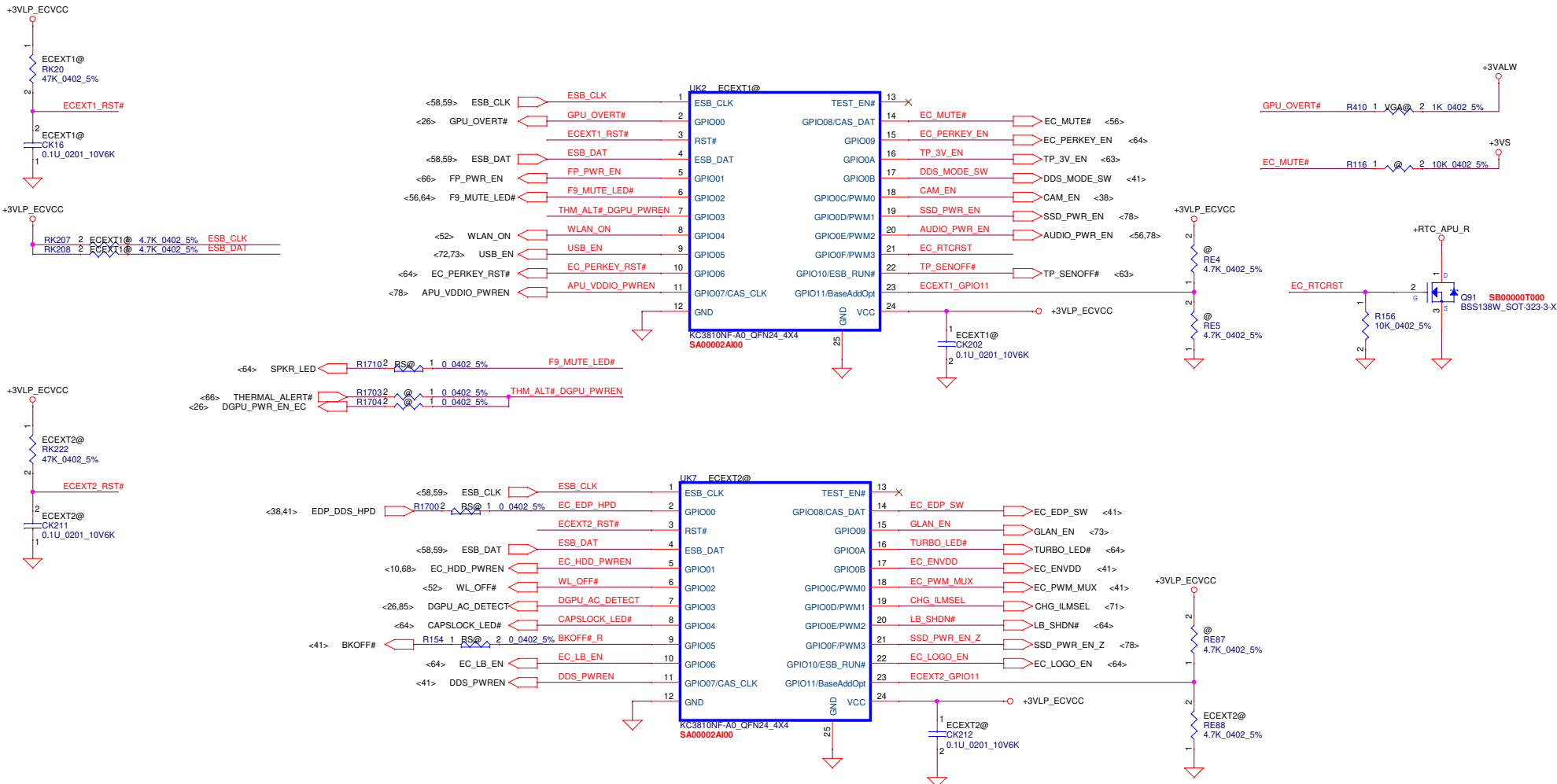
JD1	
HP-JD	LINE1-JD
200K	100K

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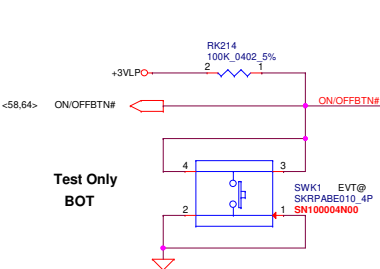
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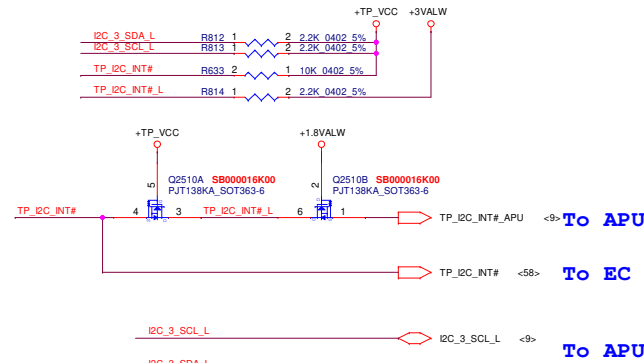
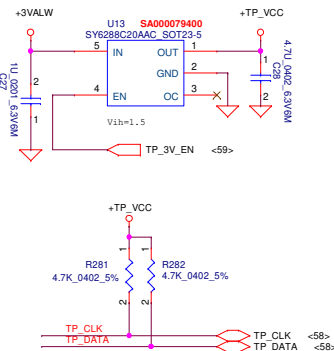
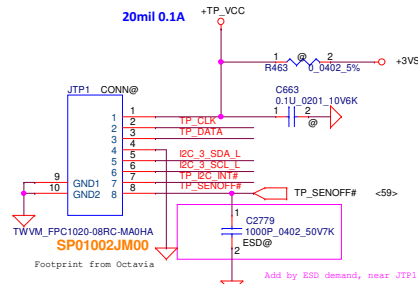
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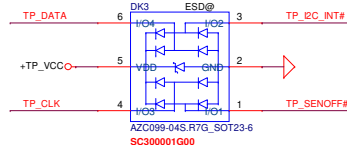
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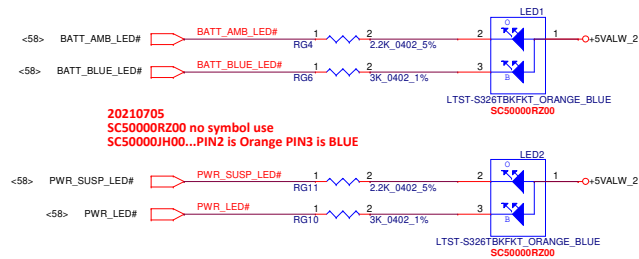
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Lid Switch (Hall Effect Switch)

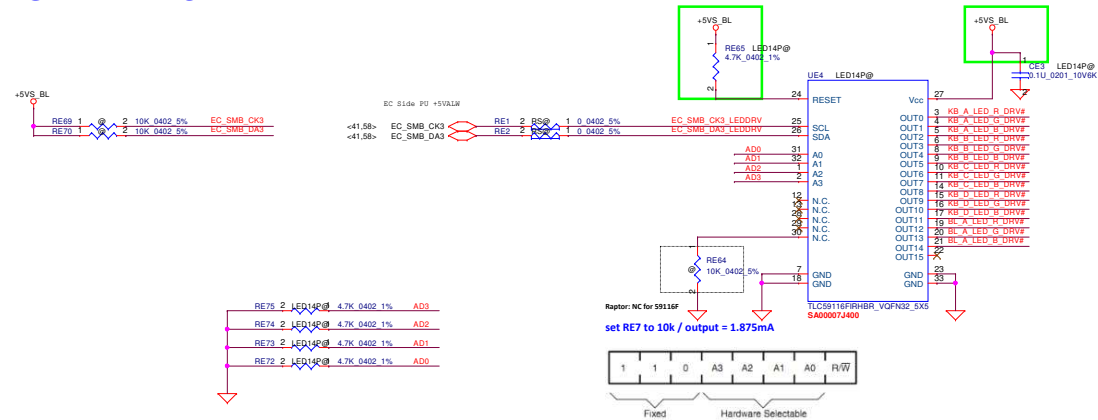


Battery LED/Power LED

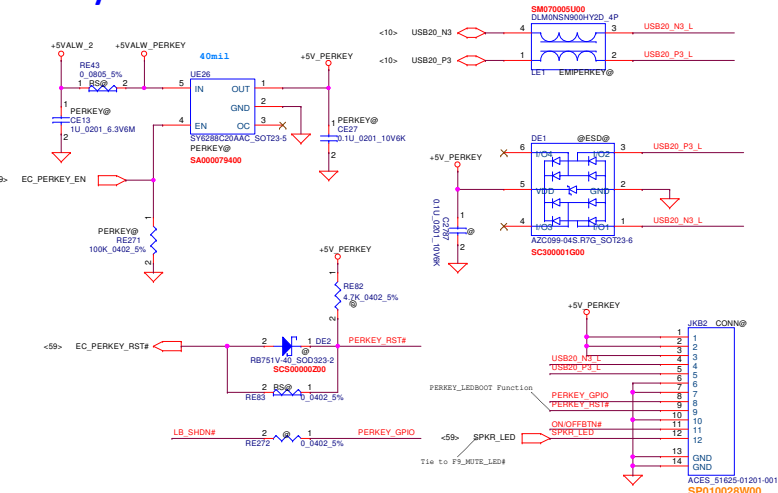


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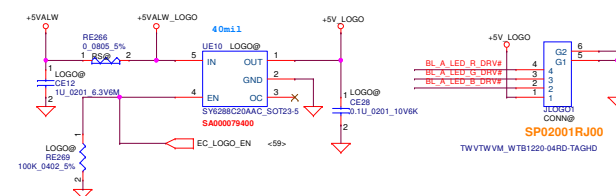
RGB LED Driver



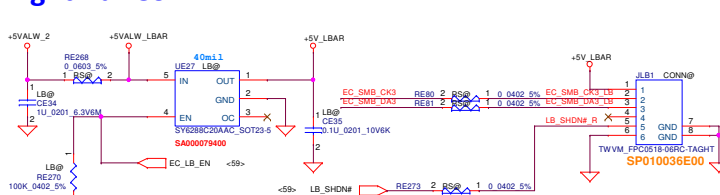
Per Key Conn.



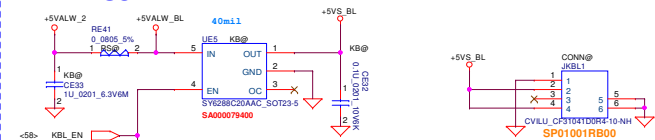
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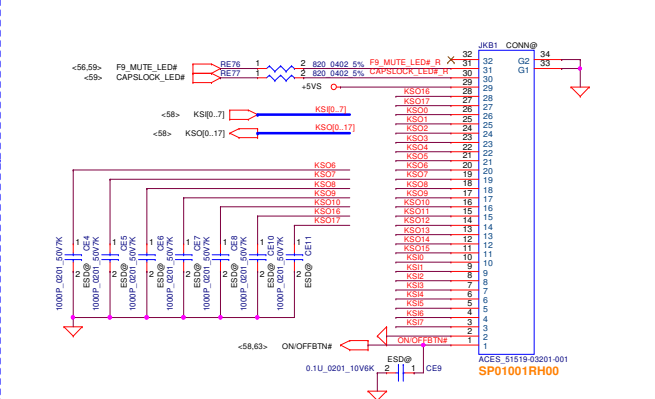
Light Bar Conn.



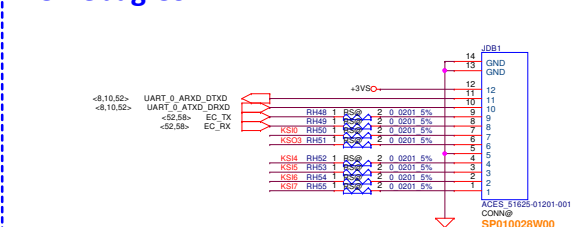
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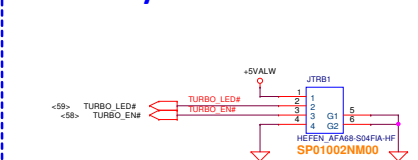
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EC Debug Conn.



Turbo Key

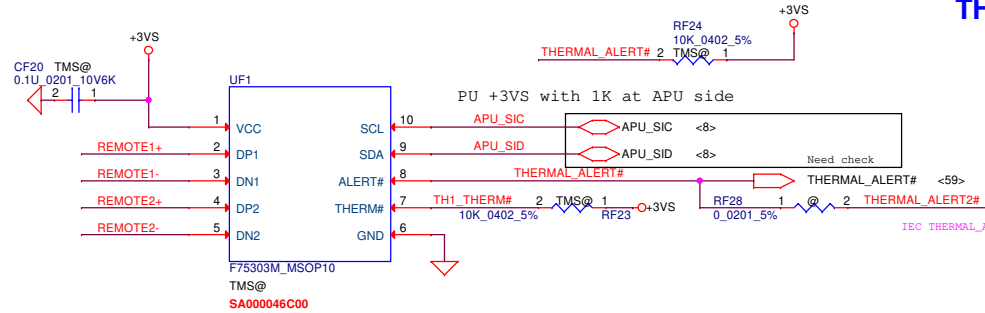
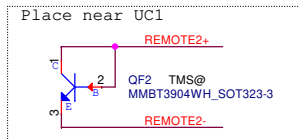
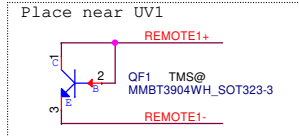
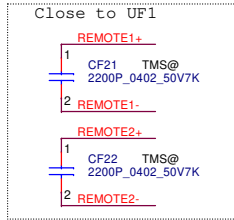


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				Sheet	64 of 122

Reserve

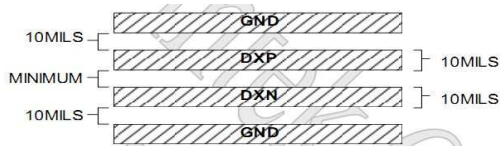
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THERMAL SENSOR

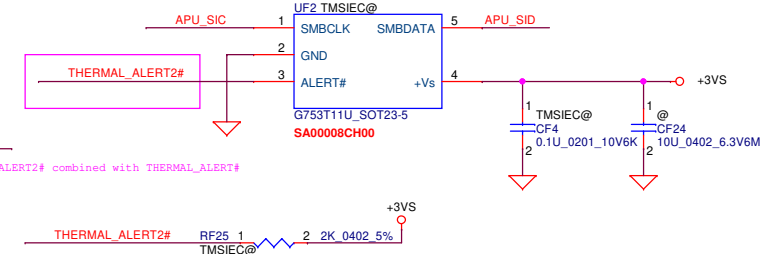


Part Number	SMBus Address
F75303M	1001_101xb

REMOTE1,2 (+/-):
Trace length: <8"



THERMAL IEC



The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

The G753 also responds to the SMBus Alert Response slave address (see the Alert Response Address section).

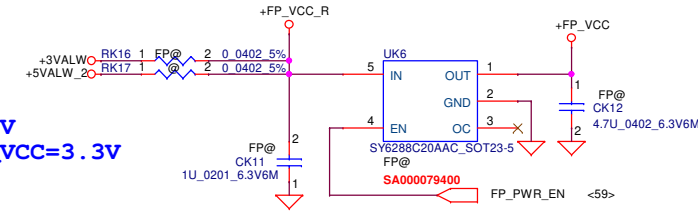
ALERT# point hardware power-on setting

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

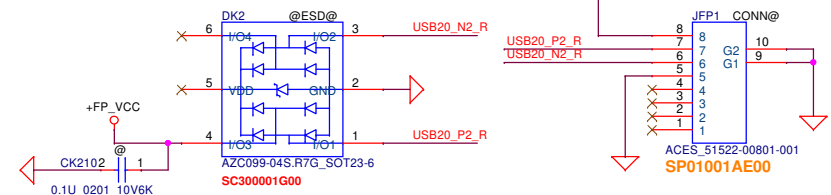
PULL-UP RESISTOR	TEMPERATURE (°C)
2kΩ	75
7.5kΩ	90
10.5kΩ	100
14kΩ	105
18.7kΩ	110

Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



PIN	SA464K-2200
1	+FP_VCC (3V)
2	D+
3	D-
4	GND
5	NC
6	NC
7	NC
8	NC

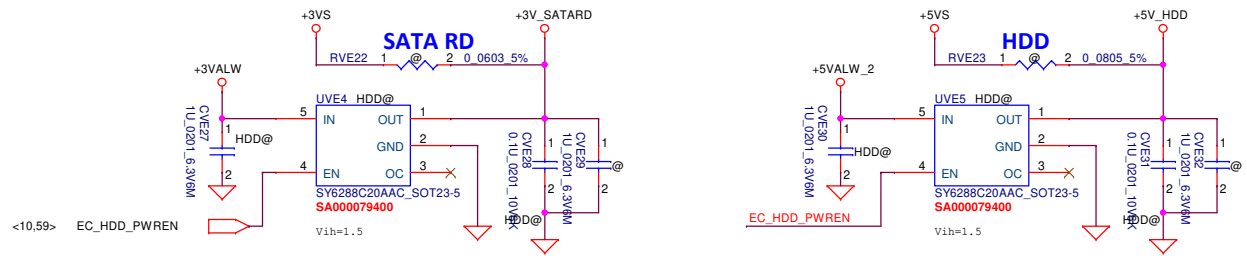
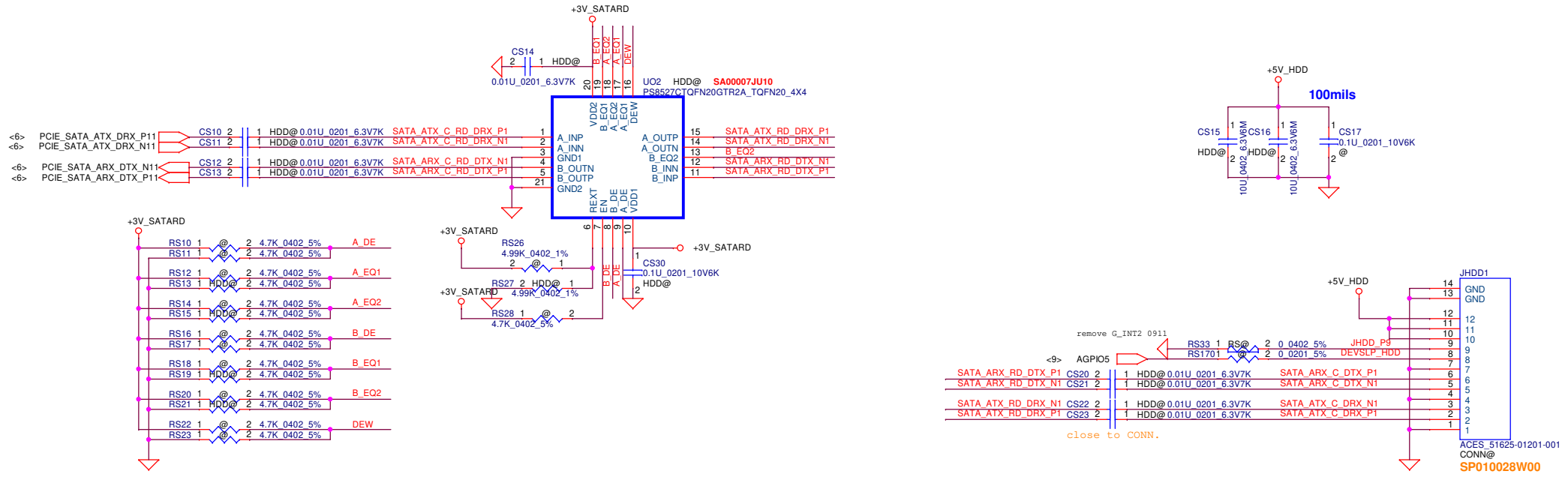


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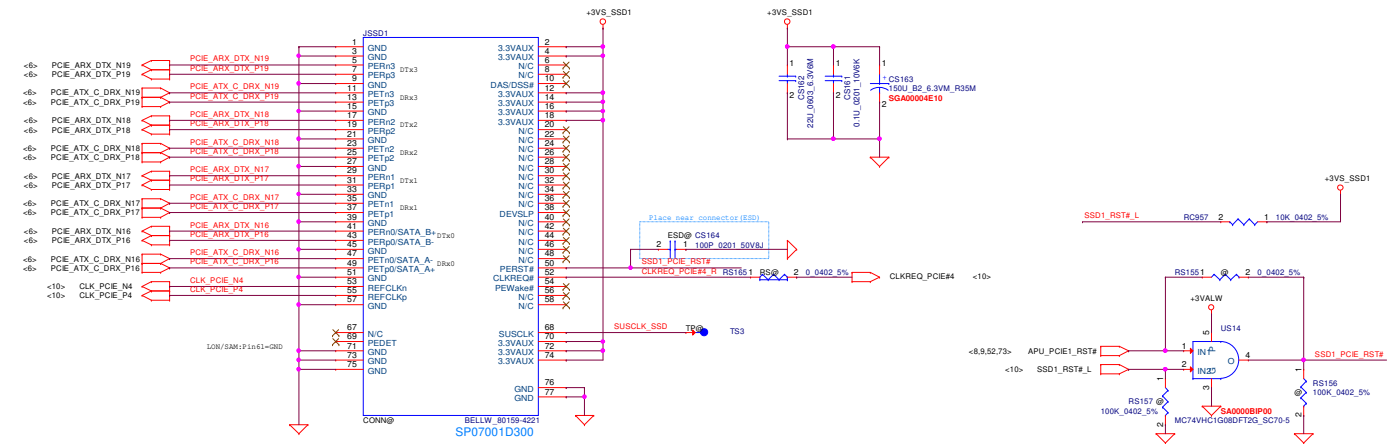
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SATA Re-Driver



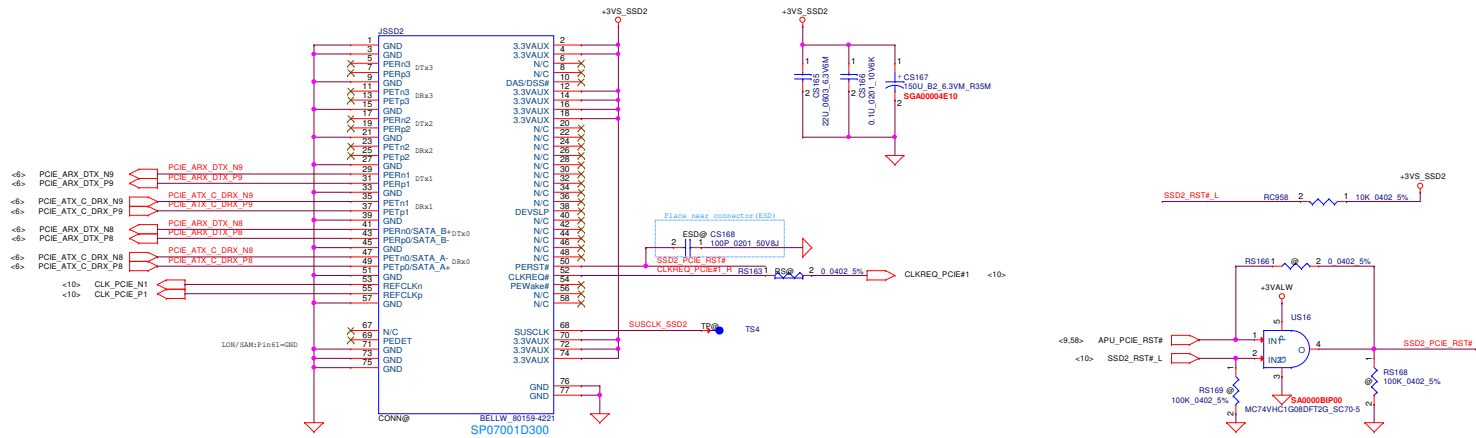
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						Size	Document Number	Rev	
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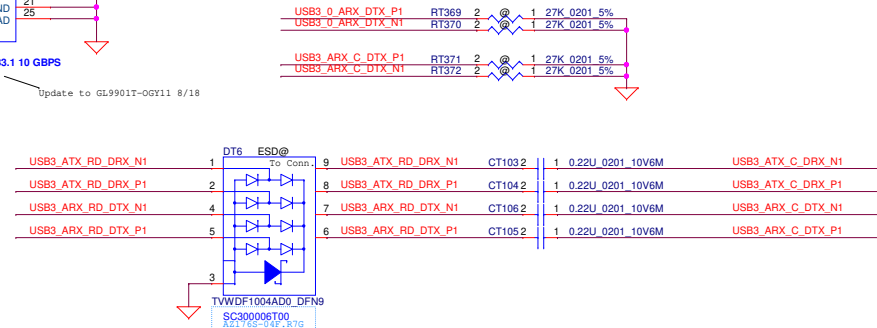
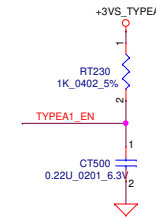
PCIE SSD x4 Conn. (R)



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PCIe SSD x2 Conn. (L)

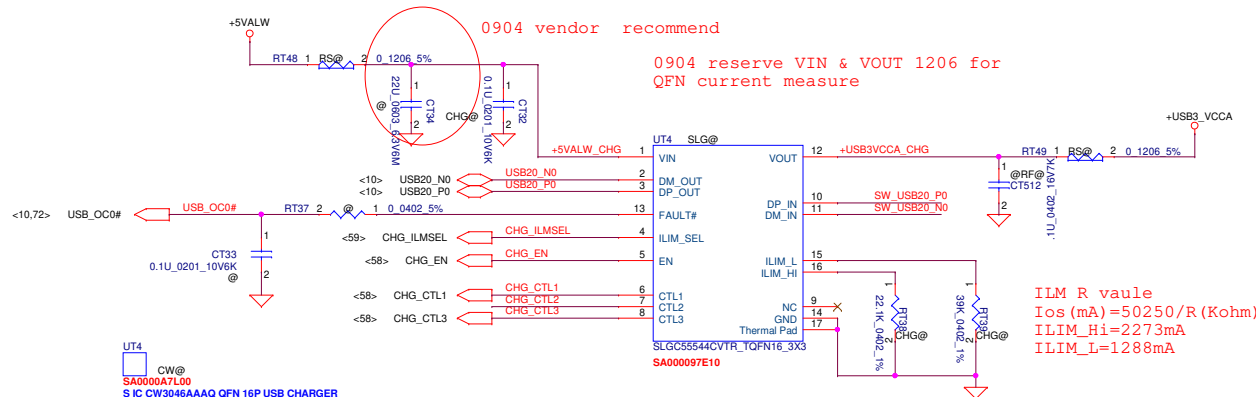
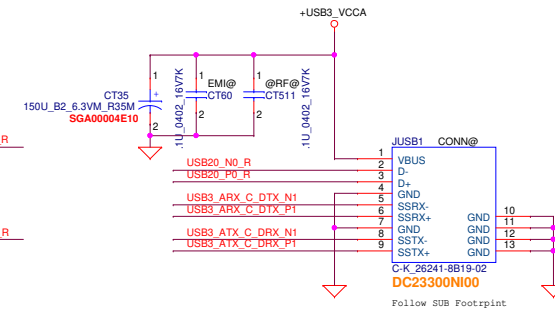




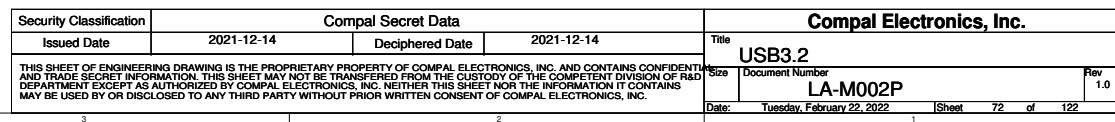
2	3	4	15	17	16	14
SW1	EQ1	DG1	SW2	EQ2	DG2	PS
F	F	F	F	F	F	H

USB Host Charger Truth Table

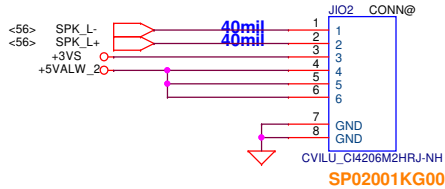
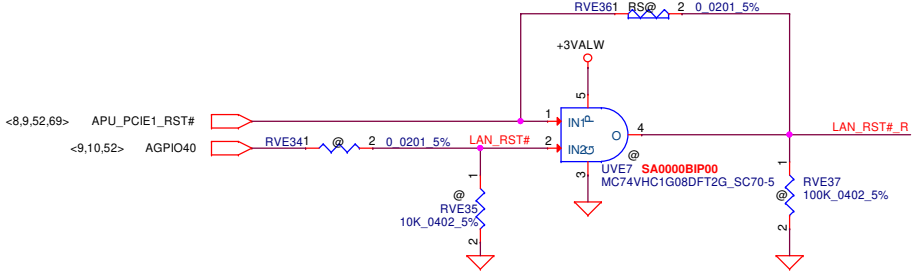
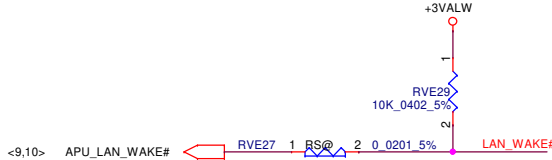
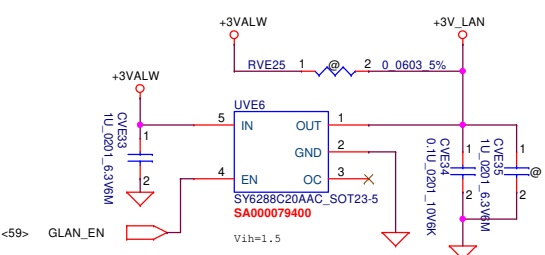
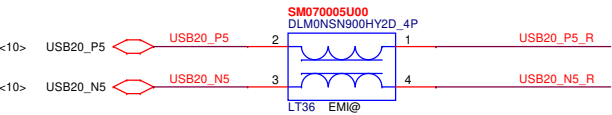
CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected



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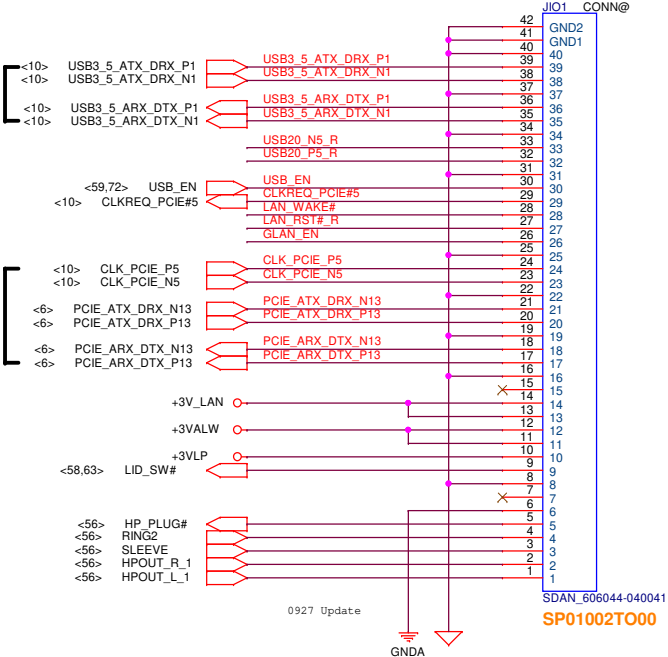


USB3.0 (Port 3)



Port 5

LAN E2600



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Date: Tuesday, February 22, 2022		Sheet 74 of 122			

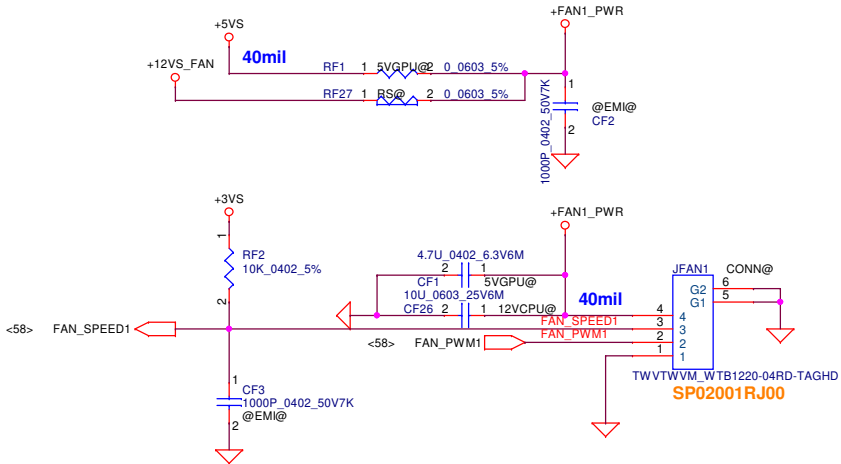
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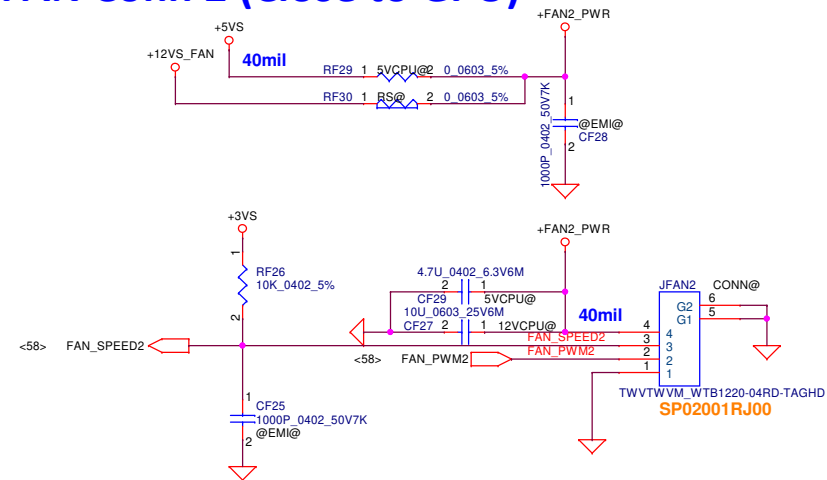
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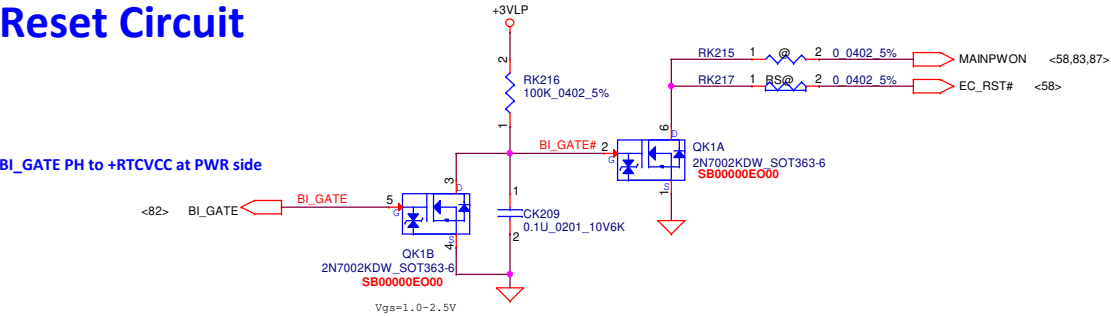
FAN Conn 1 (Close to CPU)



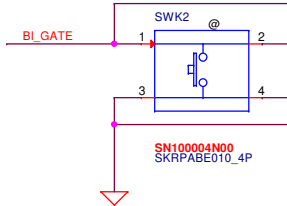
FAN Conn 2 (Close to GPU)



Reset Circuit

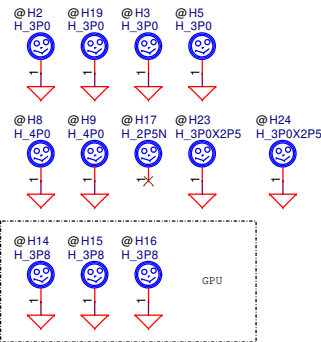


Reset Button

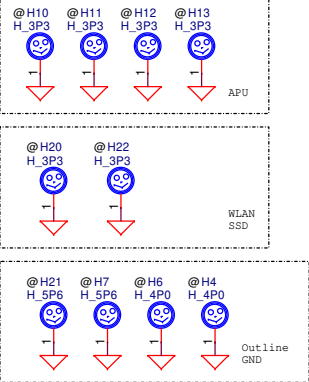


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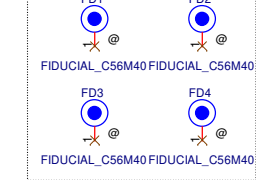
Screw Hole



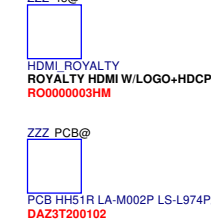
Stand OFF



Fiducial Mark



HDMI ROYALTY/PCB



DAB000AD11A, PCB 3T2 LA-M002P REV1A MB 2
DAB000AC01A, PCB 3SY LS-L974P REV1A IO/B
DA2001CW010, PCB 3SY LS-L973P REV1 KB/B

CLIP



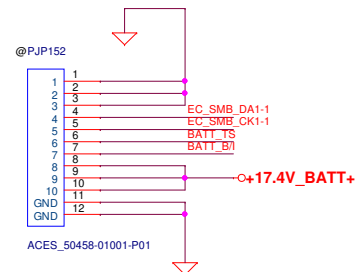
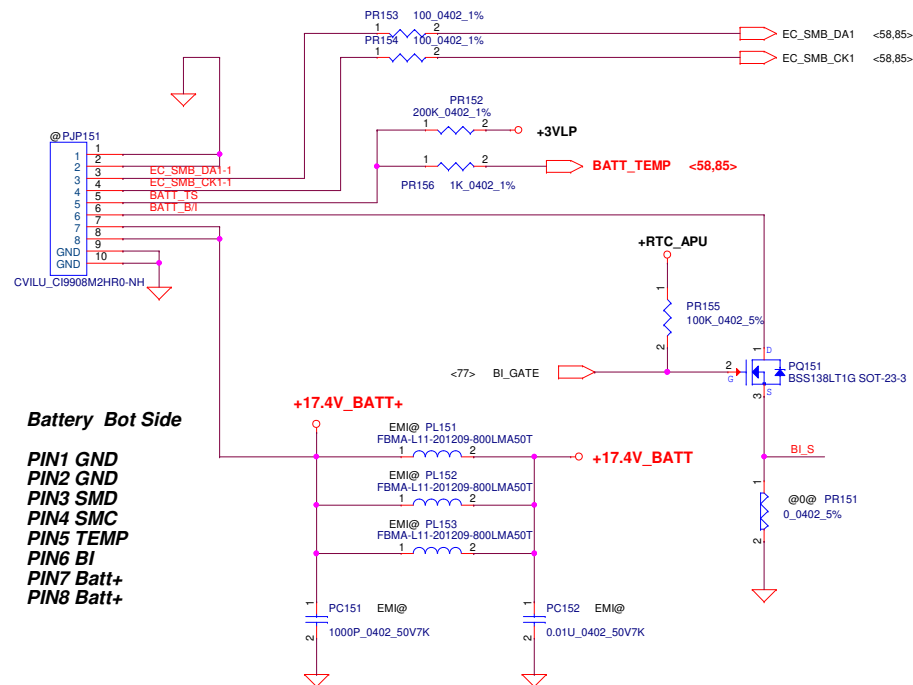
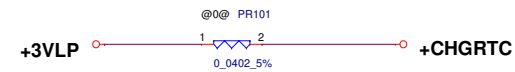
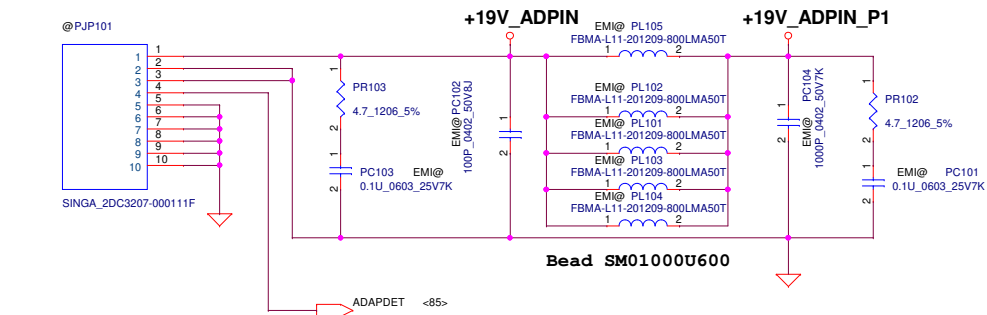
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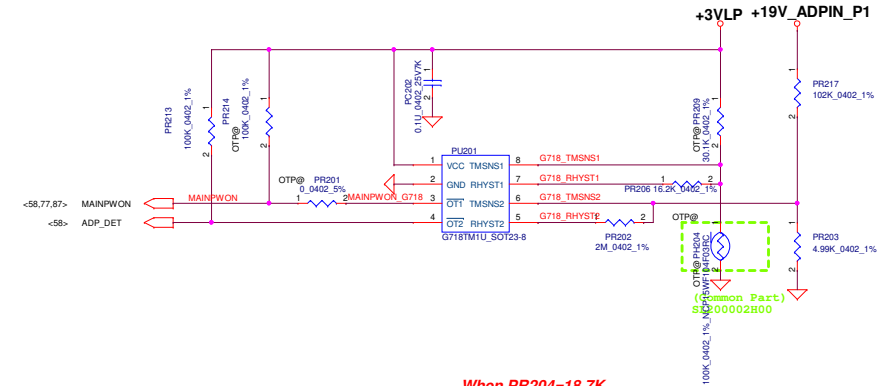
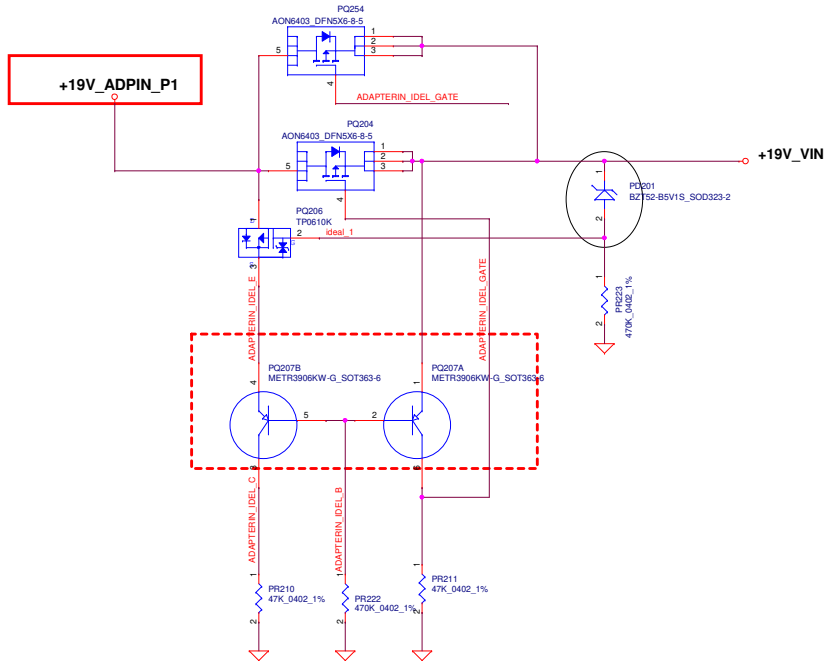
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Battery Bot Side

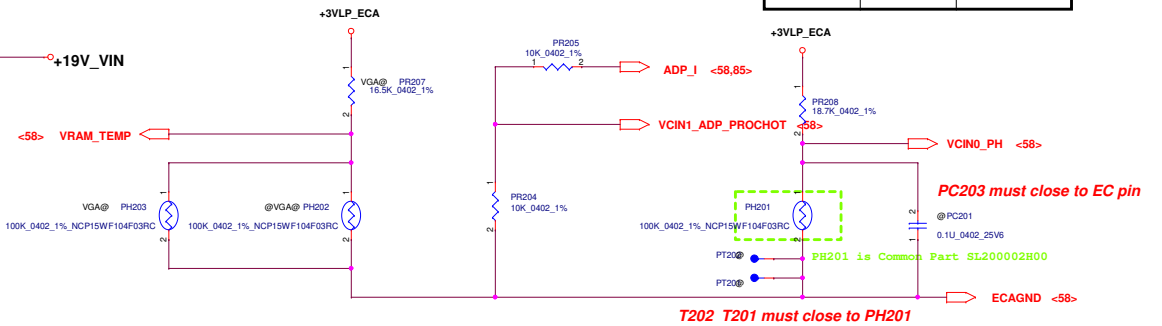
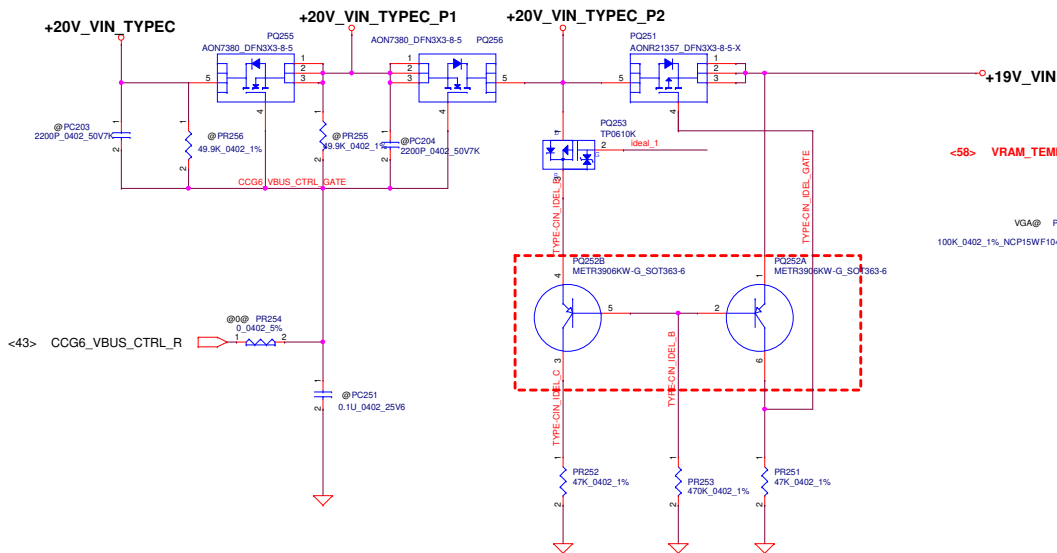
PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+

Security Classification				Compal Secret Data				Compal Electronics, Inc.			
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When PR204=18.7K

For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	89°C, 1V	56°C, 2V
PH202 (ohm)	8.0524K	26.11K



$$ADP_I = 20 * I(\text{adapter}) * 0.01$$

$$I(\text{adapter}) = \text{adapter}(W) * 130\% / 19$$

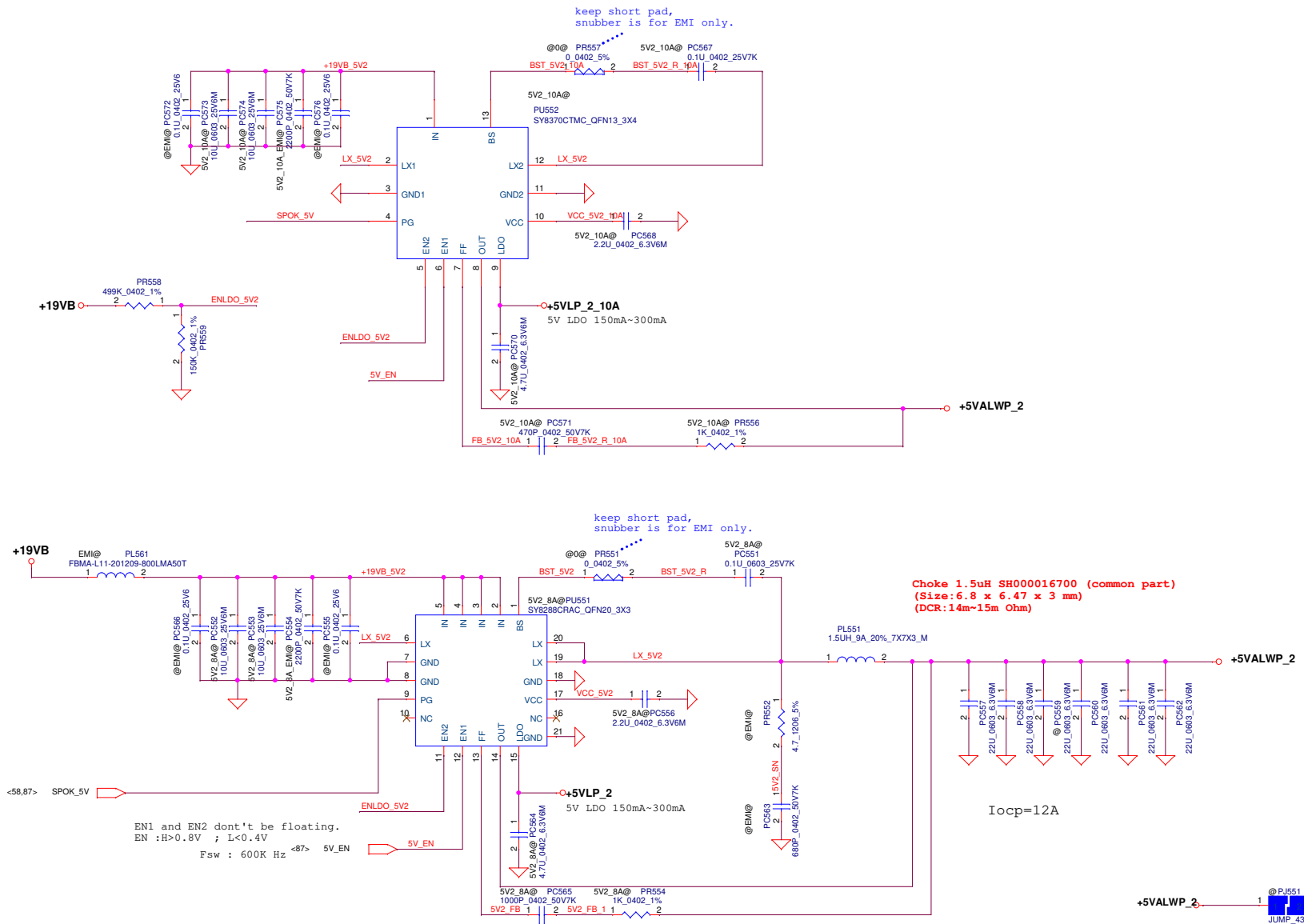
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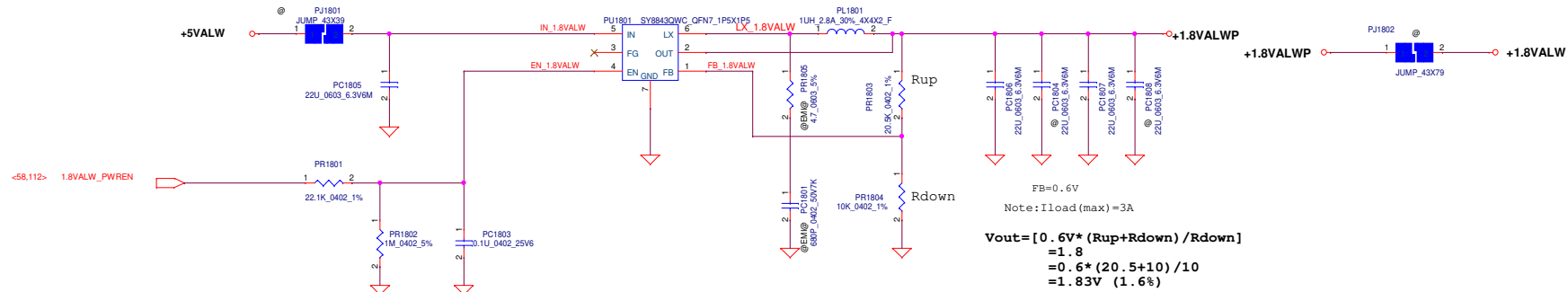
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Issued Date	2021-12-14	Deciphered Date	2021-12-14	Title	Reserve
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				Date: Tuesday, February 22, 2022	Rev 0.3
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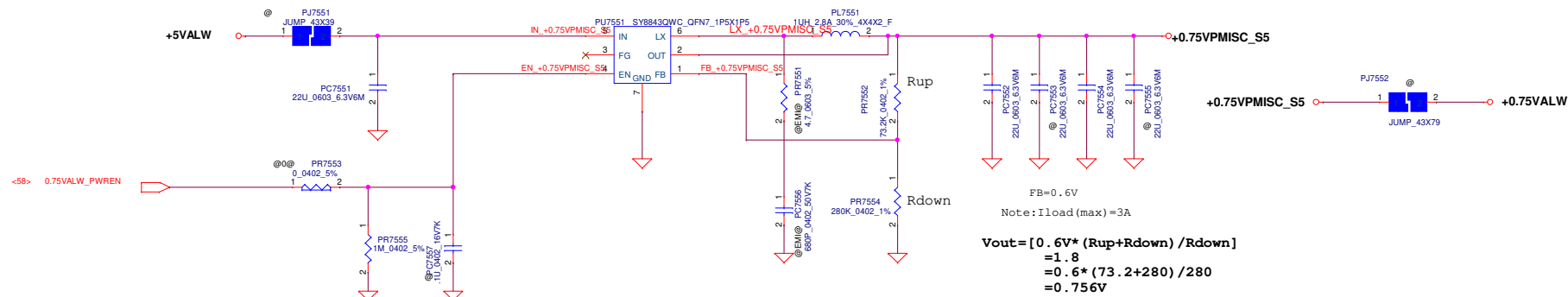
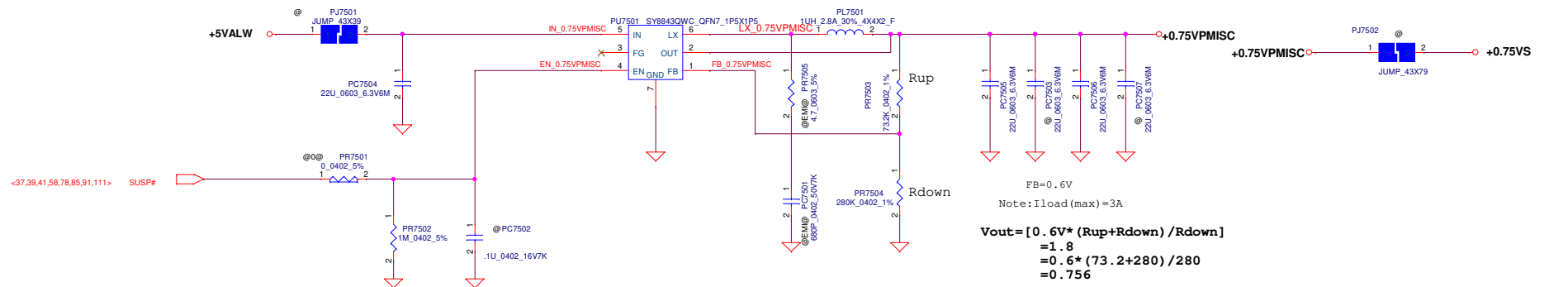
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Issued Date	2021-12-14	Deciphered Date	2021-12-14	Title +3VALW/+5VALW		
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Issued Date	2021-12-14	Deciphered Date	2021-12-14	Title	1.5VS/2.5V
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				Document Number	LA-M002P
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Issued Date		2021-12-14		Deciphered Date		2021-12-14		Title 1.8VALW					
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								Customer		LA-M002P		0.3	
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Issued Date	2021-12-14	Deciphered Date	2021-12-14	Title	LA-M002P	
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				C	1.0VS_VCCIO	0.3
				Date:	Tuesday, February 22, 2022	Sheet 96 of 122

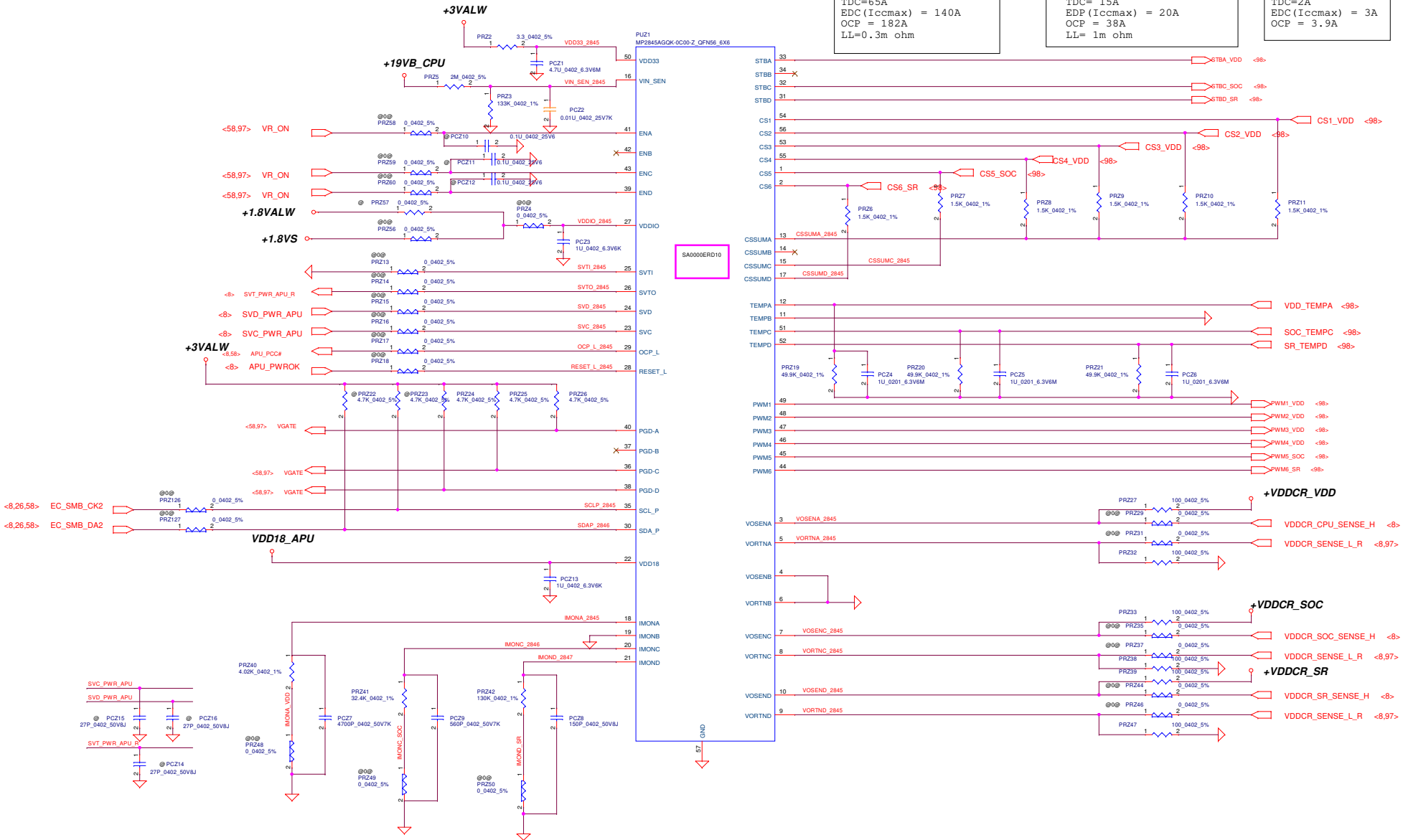
Main Func = VDDCR_VDD / VDDCR_SOC / VDDCR_SR

MPS AMD Rembrandt 54W Phase Configure:4+1+1

VDDCR_VDD
Fsw = 600 kHz
TDC=65A
EDC(Iccmax) = 140A
OCP = 182A
LL=0.3m ohm

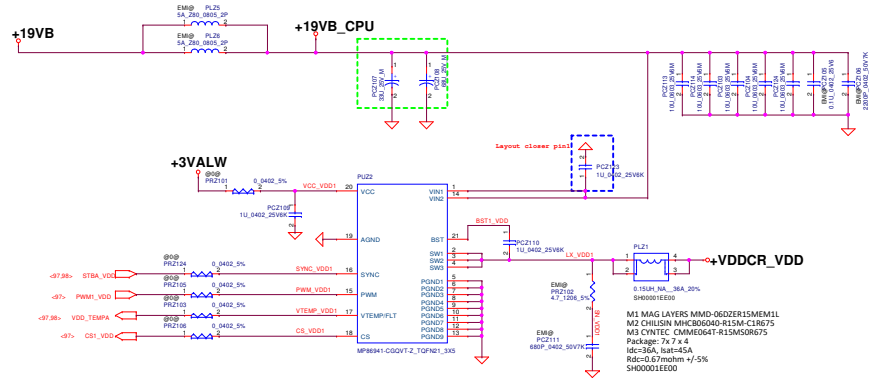
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Fsw = 600 kHz
TDC= 15A
EDP(Iccmax) = 20A
OCP = 38A
LL= 1m ohm

VDDCR_SR
Fsw = 600 kHz
TDC=2A
EDC(Iccmax) = 3A
OCP = 3.9A

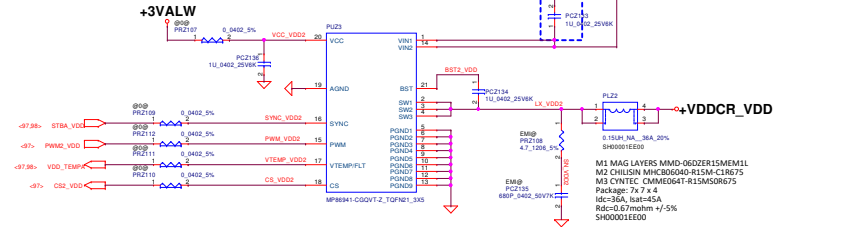


Main Func = CPU_CORE_SW

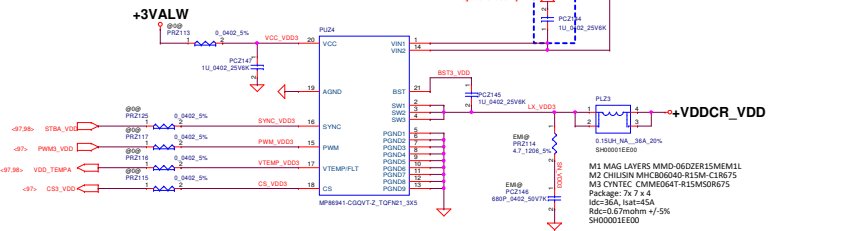
+VDDCR_VDD
TDC= 65A
EDC= Peak Current 140A



+19VB_CPU

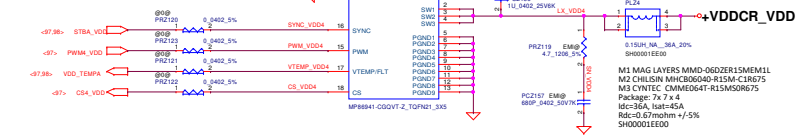


+19VB_CPU



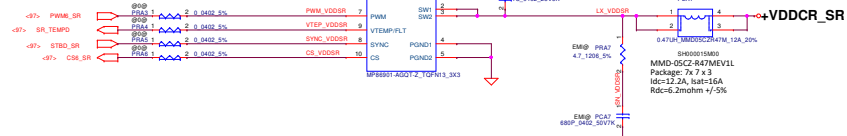
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+3VALW



+19VB_CPU

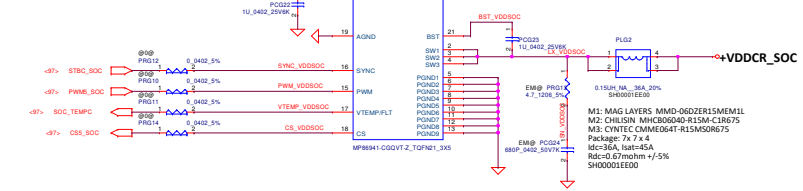
+3VALW



+VDDCR_SR
TDC= 2 A
EDP= Peak Current 3 A

+19VB_CPU

+3VALW



+VDDCR_SOC
TDC= 15 A
EDP= Peak Current 20 A

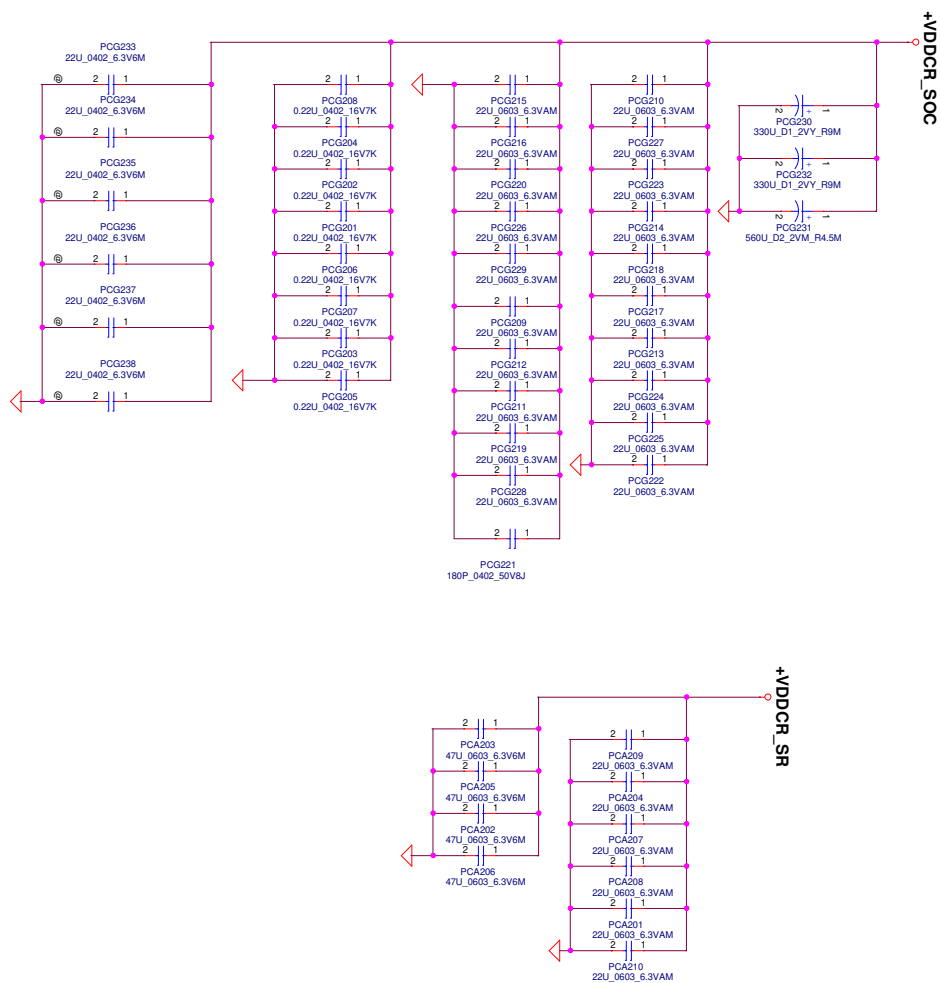
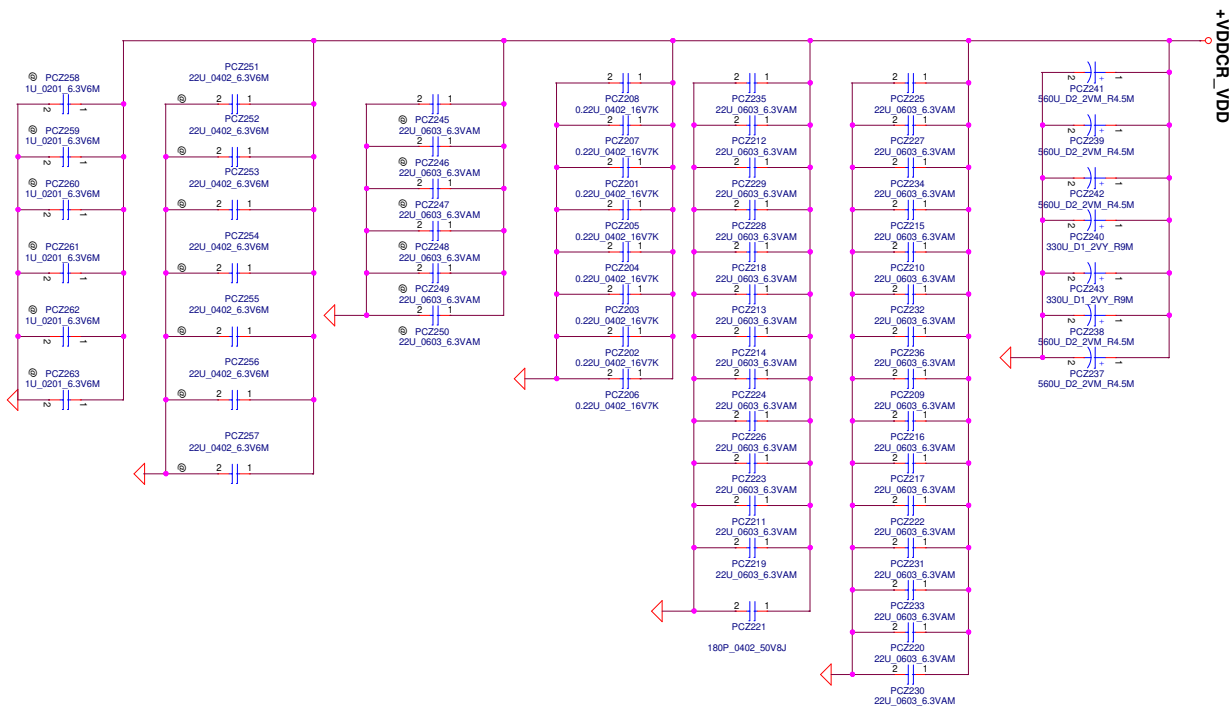
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Issued Date	2021-12-14	Disciplined Date	2021-12-14	Rev	
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Doc No	Document Number	Rev	0.1		
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				LA-M002P	0.3
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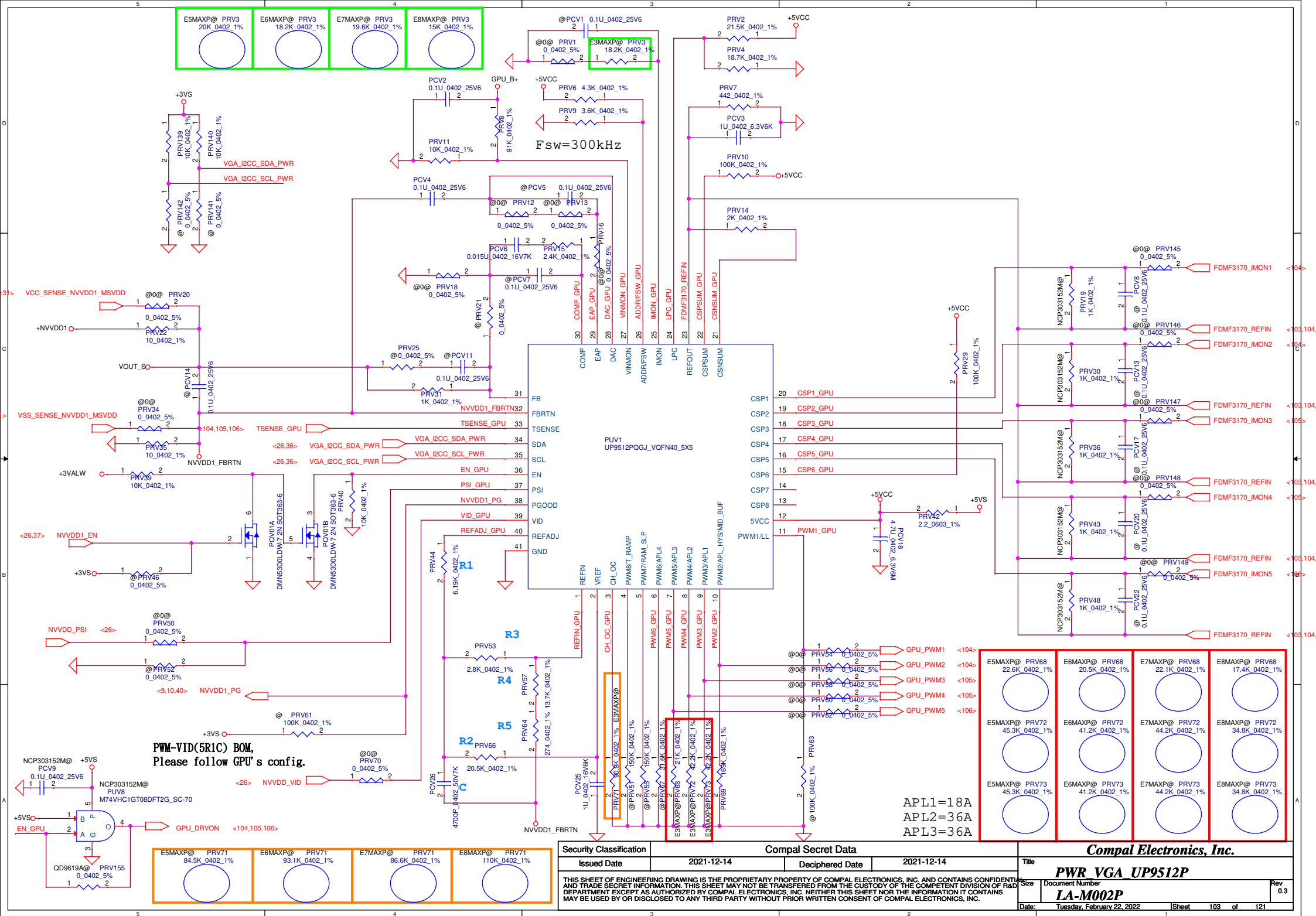
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				Date: Tuesday, February 22, 2022	Sheet 100 of 122

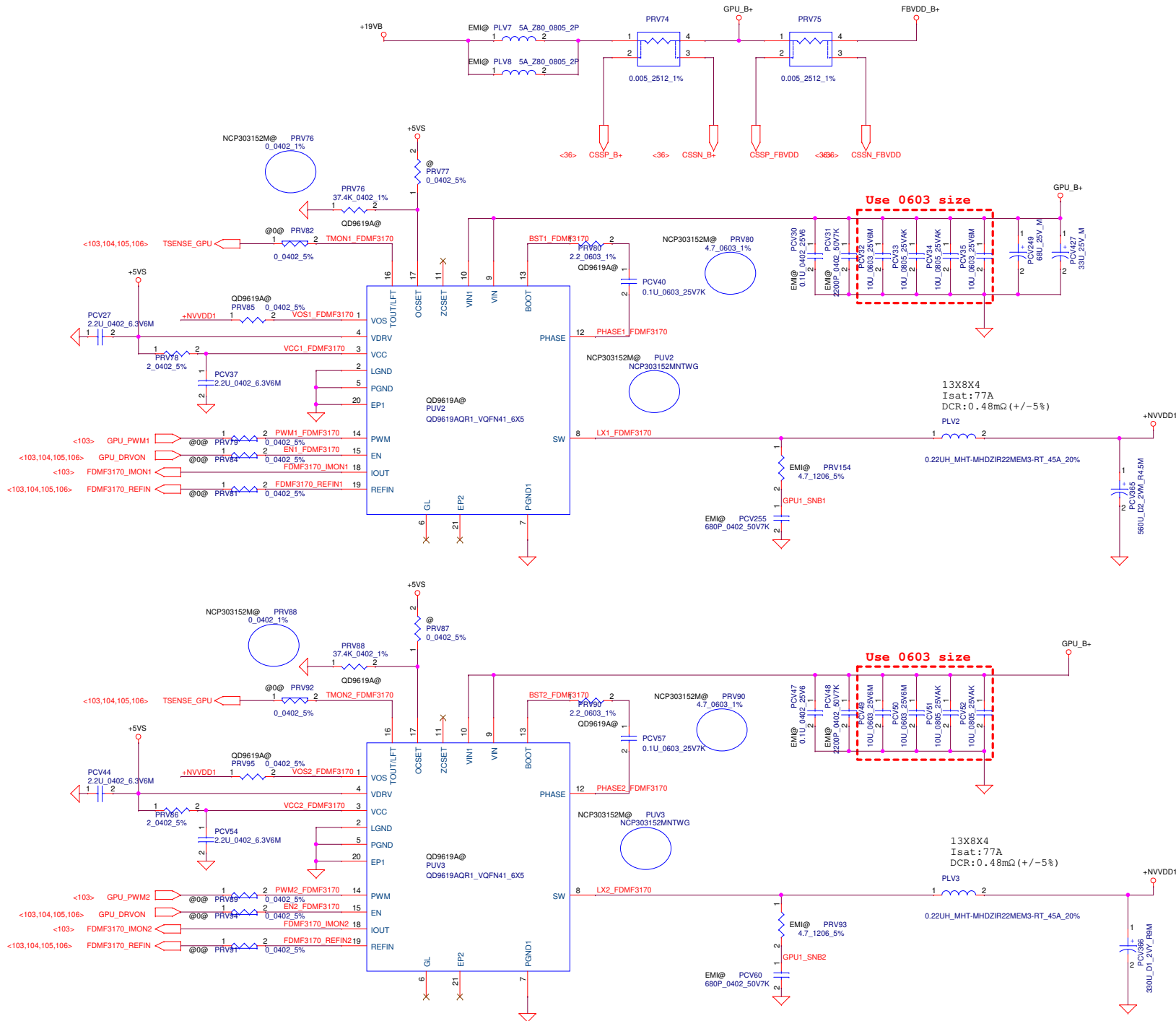


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LA-50002P		1A-50002P		0.3	
Date	1/26/2022	Sheet	101	of 122	

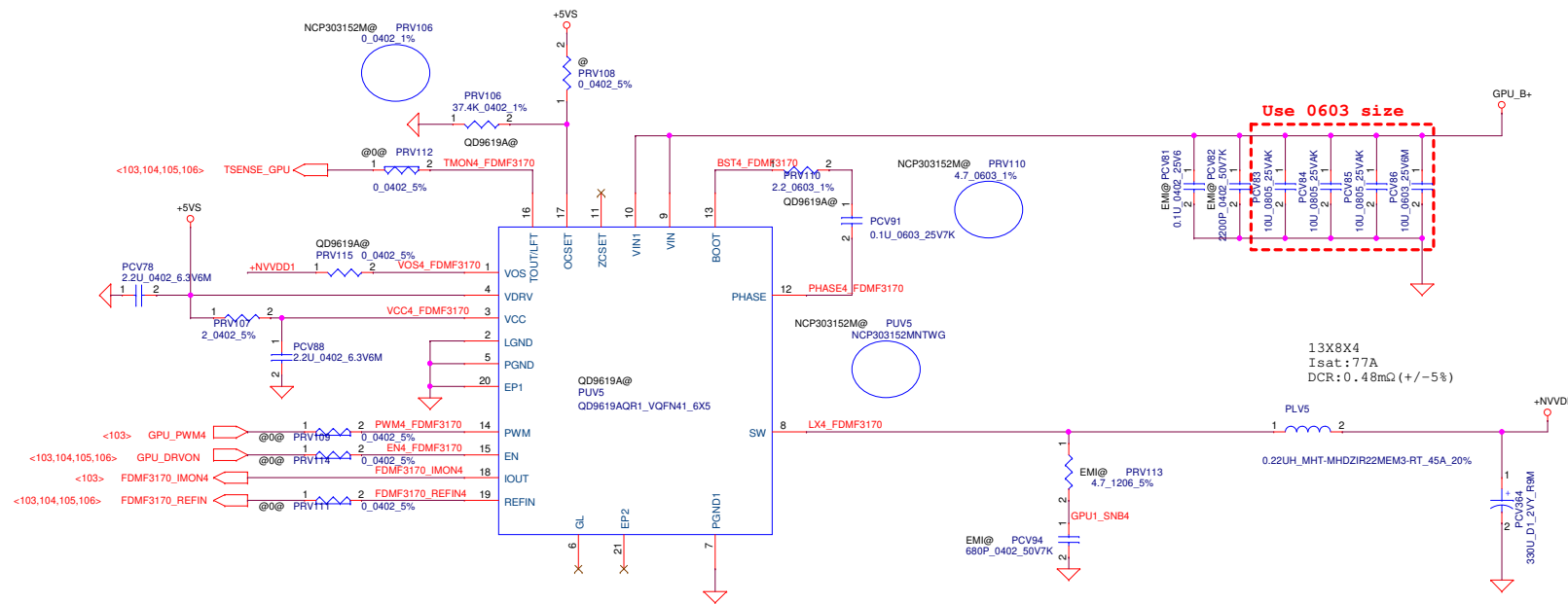
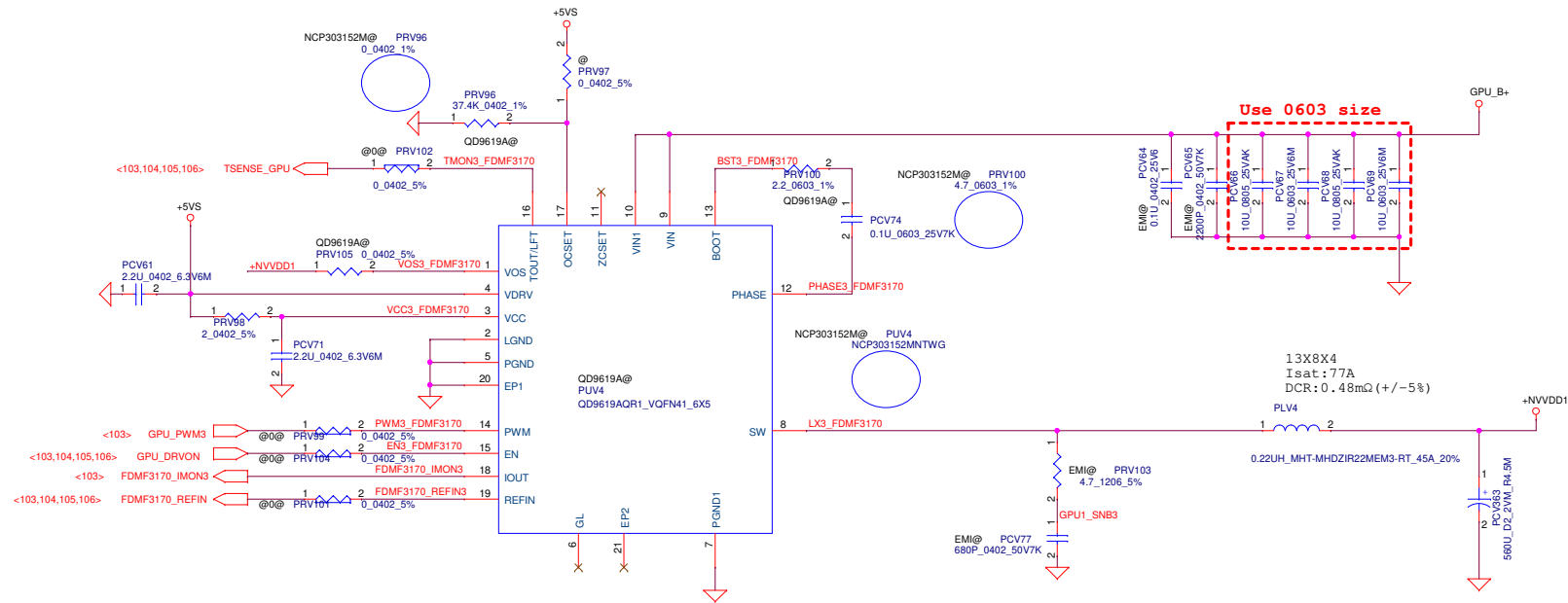
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				C	1.0VS_VCCIO	0.3
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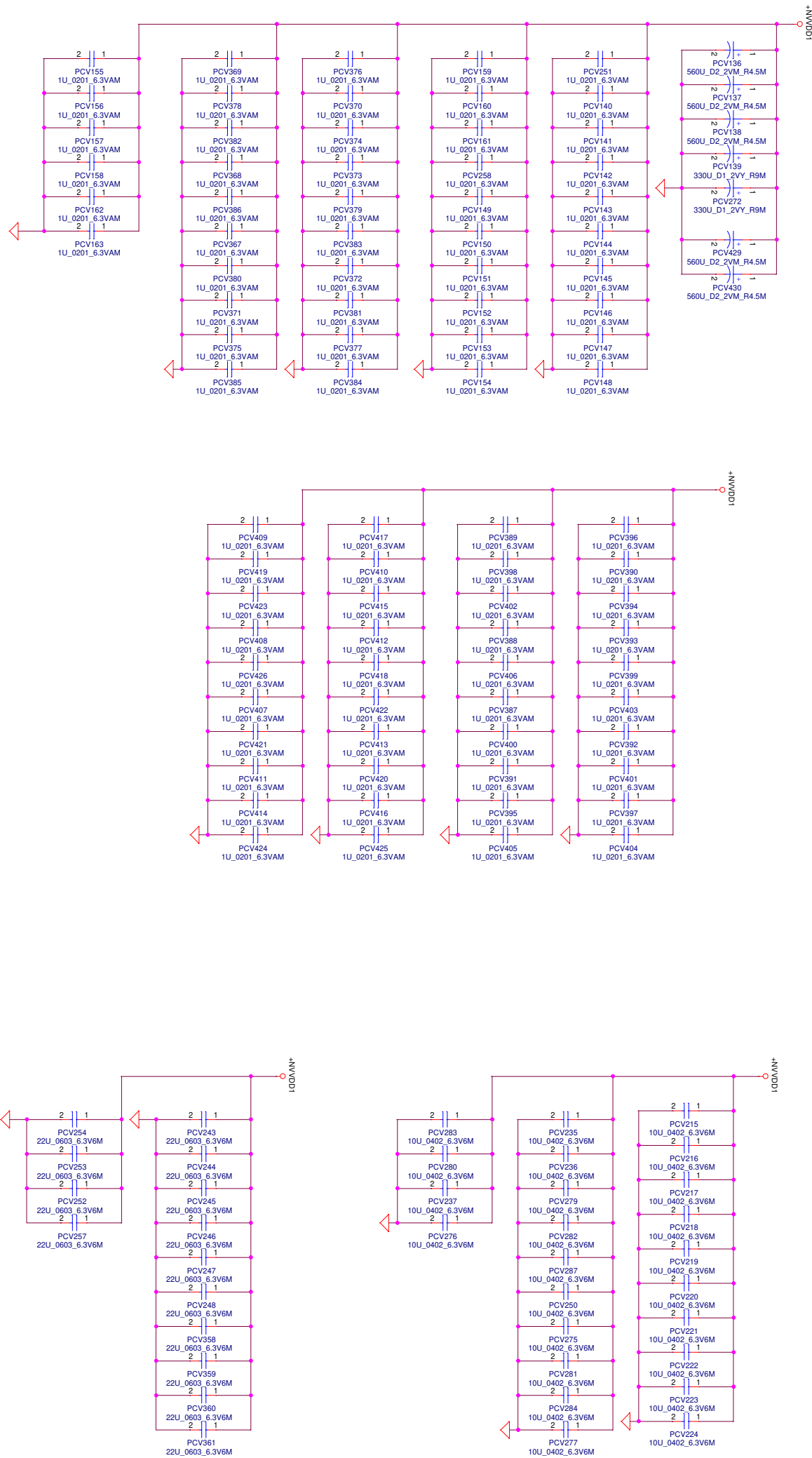




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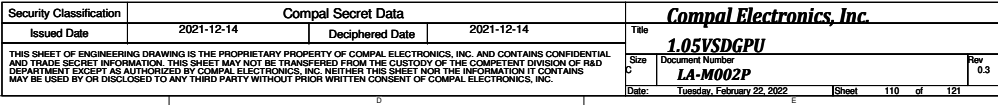


+NVDD1
560uF X 6
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28 (13+15)

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Issued Date	2021-12-14	Deciphered Date	2021-12-14	Title	
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				Document Number	
				Custom	
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HW Schematic Change List

Item	Rev.	Change Description
1	0.1	2021/09/01 First Release
2	0.2	09/01_Schematic modify - Combine PWR for SOC Power MOS change solution
3	0.3	<p>09/06_Schematic modify - Update RTK PDC solution</p> <p>09/11_Schematic modify - R840,U261,RS157,RS169 change to unpop - RG6,RG10 change to 3k</p> <p>09/22_Schematic modify - QA12,RA93,RA94,RA92,RA91,RA89,RA90 add for DMIC/SPKR_MUTE colay - QVH4,QVH2 flip direction, and RVH68,RVH69 change to unpop - QX1 change to SB00000T000 - PDC solution change to CYPD with Retimer - R1710 add for F9_MUTE_LED# tie with SPKR_LED - R154,R1700,R712,RA14,RC905,RC910,RC919,RE1,RE2,RE80,RE81,RV505,RW38,RC949,RD247 ,RD249,RV3691,RV3692,RV3693,RV3694,RV592,RVE27 change to R-short - RT102 add for reserve</p> <p>09/28_Schematic modify - OVRM Sync Intel 60 resistor - CV627 change to RV627 for correction</p> <p>10/01_Schematic modify - CVE36 add ESD request for HPD common issue</p> <p>10/06_Schematic modify - L4 change to L44, and L43 change to 0402 - RE272 reserve for PERKEY Bootup Light function - Add PC PN into schematic - UV109 add DDSA3 PN - DDR_AB_PWREN reserve 3V_EN R-C circuits - Reserve SSD_PWR_EN_Z to seperate different SSD Power - RE273 reserve for LB co-lay with PERKEY function - SPKL bead change to MB</p> <p>10/07_Schematic modify - Combine PWR</p> <p>10/13_Schematic modify - RA16,RA17 change to 47ohm - RK207,RK208 change to 1k - DDR_PWR_EN change to SYSON, RD246 pop, RD250 unpop. - CT207,CT208 change to SE169391KY0 - R1705 pop,R1695 unpop for DDR power sequence - RC715 add HH51R60@, RC716 add HH51R50@ - Update EC Board ID at NOTE LIST - R1698 add PERKEY@,R1699 add NPERKEY@ - R1697 add SLG@,R1696 add CW@</p> <p>10/14_Schematic modify - RK207,RK208 return to 4.7k - RE88 change to 4.7k</p>

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HW Schematic Change List

Item	Rev.	Change Description
4	1.0	<p>11/16_Schematic modify</p> <ul style="list-style-type: none"> - QVD1 change to SB00000T000 (Sync source) - UT39 change to SA0000DVV00 (Sync source) - R778 change to SD034100380 (60DVT@ source shortage) - RG4,RG11 change to SD028220180 (2.2kohm) - LED1,LED2 update PCB footprint (Sync with Intel) - RV700,RV702,RV703,RV704,RV705,RV706,RV707,RV708 change to SD000023200 (5.6ohm for HDMI2.1 Impedance) - RV789 add to reserve blackscreen issue - RV812 add to reserve APU path direct to Connector - PERKEY_RST# change to pin9, SPKR_LED remove LB_SHDN# path. <p>11/23_Schematic modify</p> <ul style="list-style-type: none"> - RE272 add back sync with Intel <p>11/24_Schematic modify</p> <ul style="list-style-type: none"> - RA1,RA23,RA81,RA84,RA85,RA86,RVE5,RVE36,RV621,RV687,RC948,RC952,RC953 RC101,RC102,RC103,RC104,RC821,RC903,R408,RC756,RC837,RC886,RV656,RC755,RC885,RV299,RC913,RV593 RV594,RV596,RV688,RV709,RV710,RV711,RV712,RV713,RV714,RV715,RV716,RV725,RE41,RE43,RE83,RE272 RE266,RE268,RE273,RF27,RF30,RT62,RT64,RT70,RT71,RT77,RT78,RT79,RT80,RT111,RT1221,RT1222,RT1223 RT1224,RT1433,RT1434,RT220,RT876,RT1242,RT1243,RT1430,RVE63,RV24,RV699,RV114,RV115,RV178,RV120 RV370,RV401,RV415,RV507,RV529,RW12,RW32,RY1,RY2,RY3,RY4,RY5,RY6,RY7,RY8,R117,R777,R968,R1693 R384,R959 - UT4 change to SLG@,add SA0000A7L00 for CW@ - RT1436 reserve to PD. - RV812 change to pop - UC1 add 560PR@,561PR@,562PR@ PN for PR Samples - UV62 add to reserve PWM IC <p>11/26_Schematic modify</p> <ul style="list-style-type: none"> - JSKT2 footprint add -NPM for colay <p>11/29_Schematic modify</p> <ul style="list-style-type: none"> - DT30,DT31,DT32,DT33,DT34,DT35,DT36,DT37 add to reserve location - RV688,RV656,RV401,RC952,RC953,RV687 change to 0ohm <p>11/30_Schematic modify</p> <ul style="list-style-type: none"> - RT998 add +3VALW path. <p>12/03_Schematic modify</p> <ul style="list-style-type: none"> - UT5 change PN to SA0000DFA50 <p>12/14_Schematic modify</p> <ul style="list-style-type: none"> - UT40,APU,GPU PN update

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